ECOLE POLYTECHNIQUE DE BRUXELLES

Using the PROMETHEE methodology for the design of 3D-stacked integrated circuits

DOAN Nguyen Anh Vu

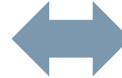
Supervisors: Yves DE SMET
Dragomir MILOJEVIC
Frédéric ROBERT

ULB beams

IMW 2014

Imagine…
The design an electronic device…

ULB



easyvhdl.vhd - HDL Editor

File Edit Search View Synthesis Project Tools Help

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity easyvhdl is
5      port (
6          DOOR: in STD_LOGIC;
7          IGNITION: in STD_LOGIC;
8          SBELT: in STD_LOGIC;
9          BUZZER: out STD_LOGIC
10     );
11 end easyvhdl;
12
13 architecture easyvhdl_arch of easyvhdl is
14 begin
15   -- <<enter your statements here>>
16
17       BUZZER <= IGNITION and ((not DOOR) or (not SBELT));
18
19 end easyvhdl_arch;
20
21
```

Design criteria

Battery life: 18h/500h
Perf: 1.7 GHz quad-core
Memory: 2GB DDR2
GPS, BT4.0, NFC, etc.
Multimedia features

CPU Qualcomm:
1.7 GHz quad-core

High-level design

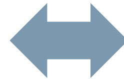
Let us focus on the design of the integrated circuit

ULB

easyvhdl.vhd - HDL Editor

File Edit Search View Synthesis Project Tools Help

```vhdl
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity easyvhdl is
5      port (
6          DOOR: in STD_LOGIC;
7          IGNITION: in STD_LOGIC;
8          SBELT: in STD_LOGIC;
9          BUZZER: out STD_LOGIC
10     );
11 end easyvhdl;
12
13 architecture easyvhdl_arch of easyvhdl is
14 begin
15   -- <<enter your statements here>>
16
17      BUZZER <= IGNITION and ((not DOOR) or (not SBELT));
18
19 end easyvhdl_arch;
20
21
```



High-level design

CPU Qualcomm:
1.7GHz quad-core

Design criteria

Battery life: 18h/500h
Perf: 1.7GHz quad-core
Memory: 2GB DDR2
GPS, BT4.0, NFC, etc.
Multimedia features

The problem is to make the right choice among the design parameters

Design criteria

- Performance
- Cost
- Consumption
- Thermal dissipation
- Size

Multicriteria considerations

Design parameters

- Architectural options
- Technological options
- Floorplanning
- Communication infrastructure

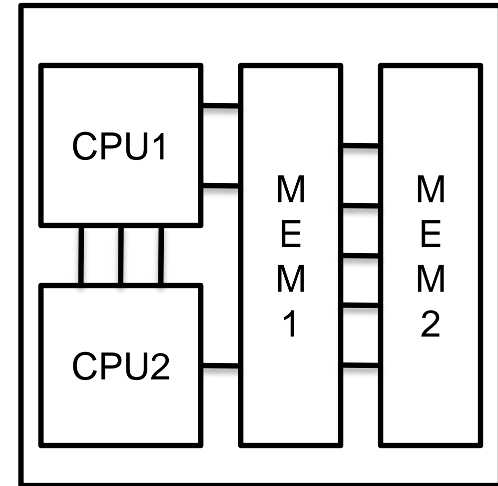
Combinatorial optimization aspects

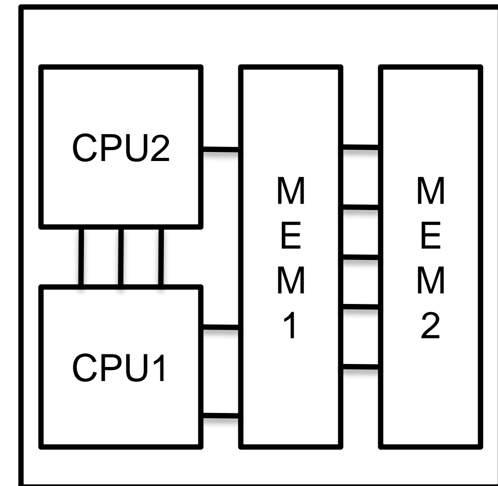
Example of the multicriteria and combinatorial optimization aspects

ULB

Criteria
- Performance
- Cost
- Consumption
- Thermal dissipation
- Size

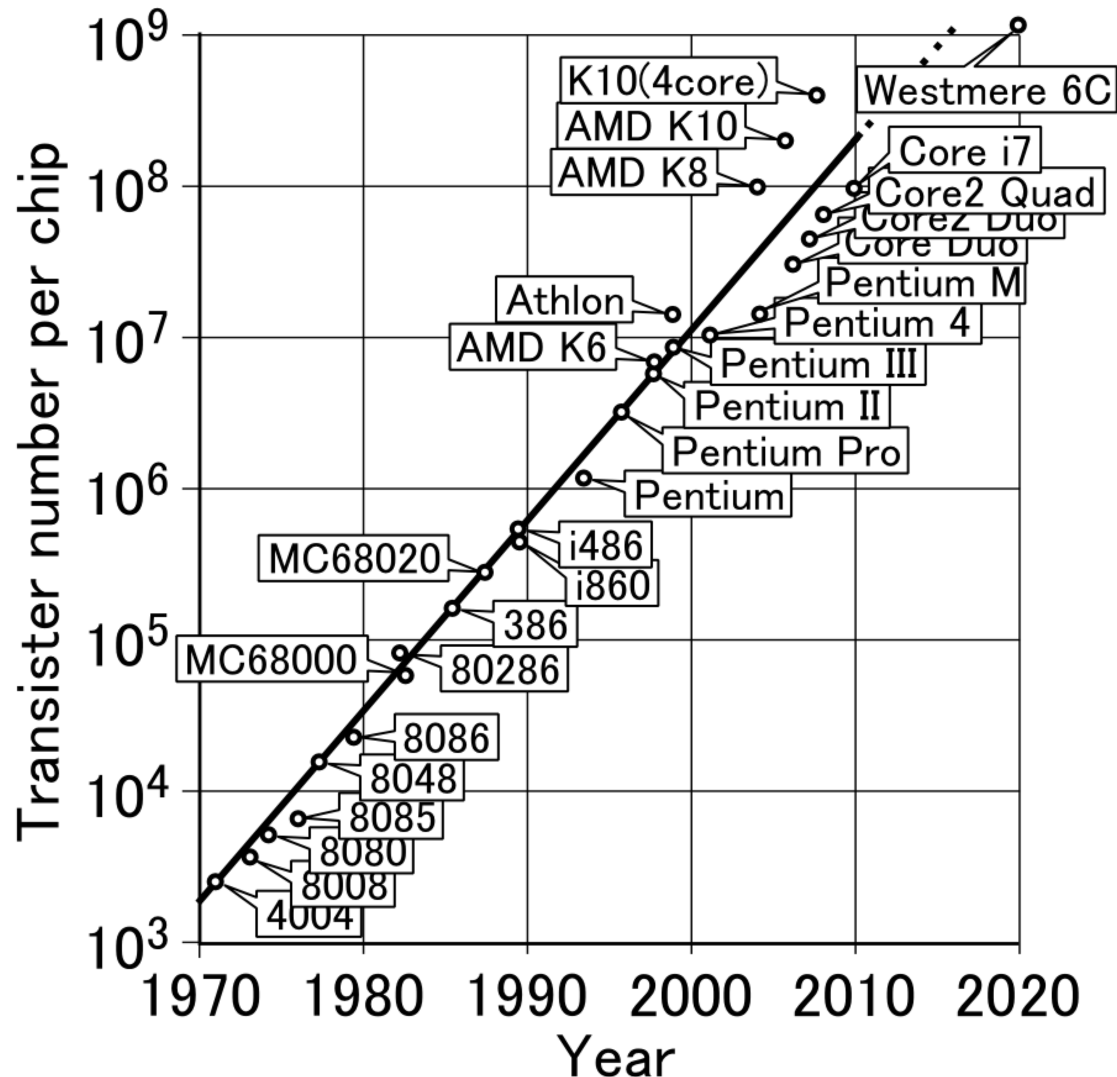
Components placement





Due to physical limitations of the silicon, it will be difficult to improve the performance

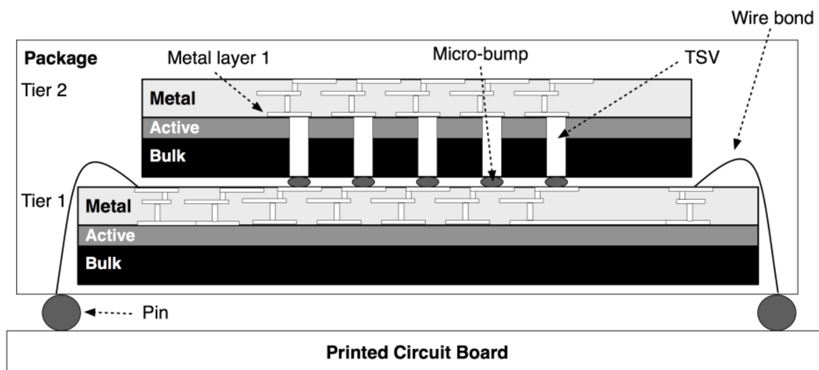
ULB

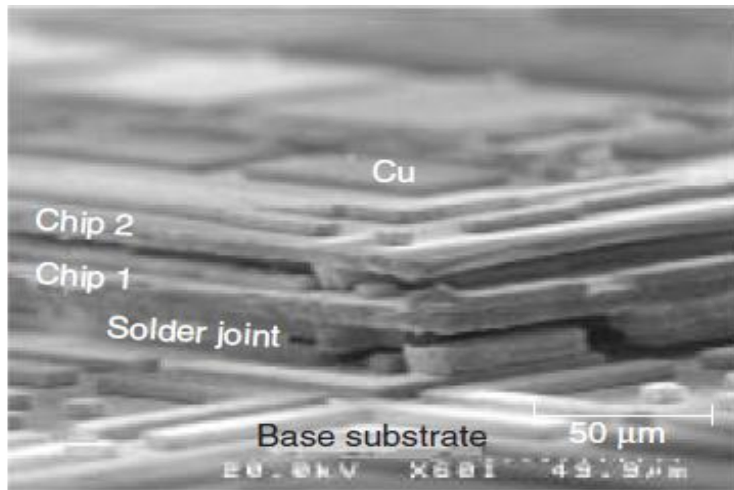


Imagine further…
The next technologies for the design

ULB

3D-Stacked Integrated Circuit (3D-SIC)



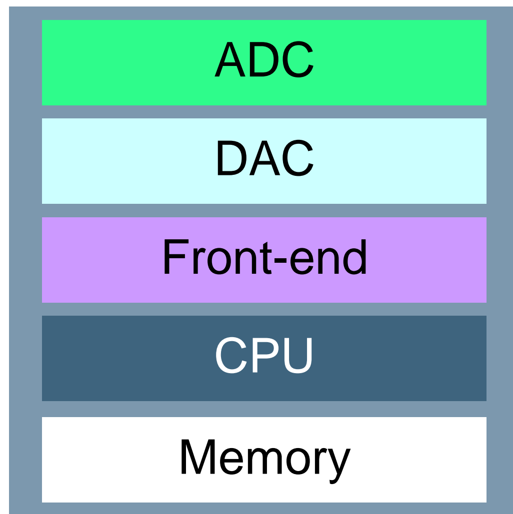


- Shorter interconnections
- Large bandwidth
- Better footprint
- Smaller packaging
- Heterogeneous circuits

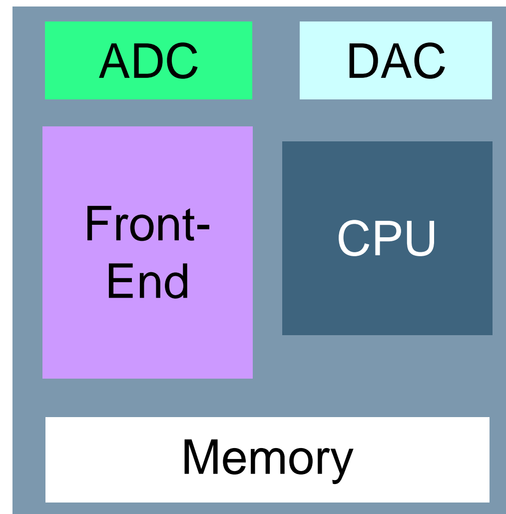
There are more design parameters when using 3D-SIC

ULB

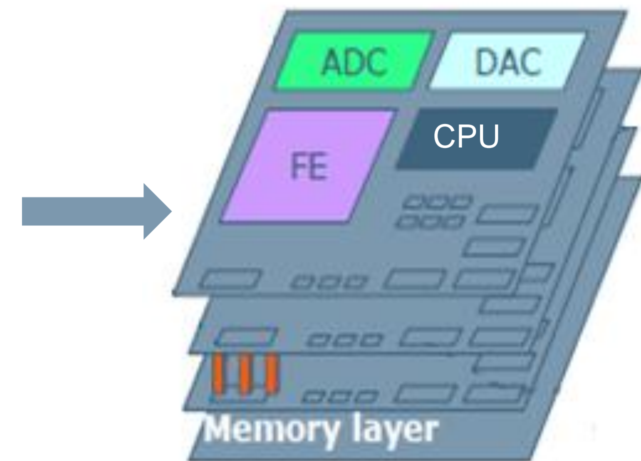
Functional specifications



2D-IC



3D-SIC

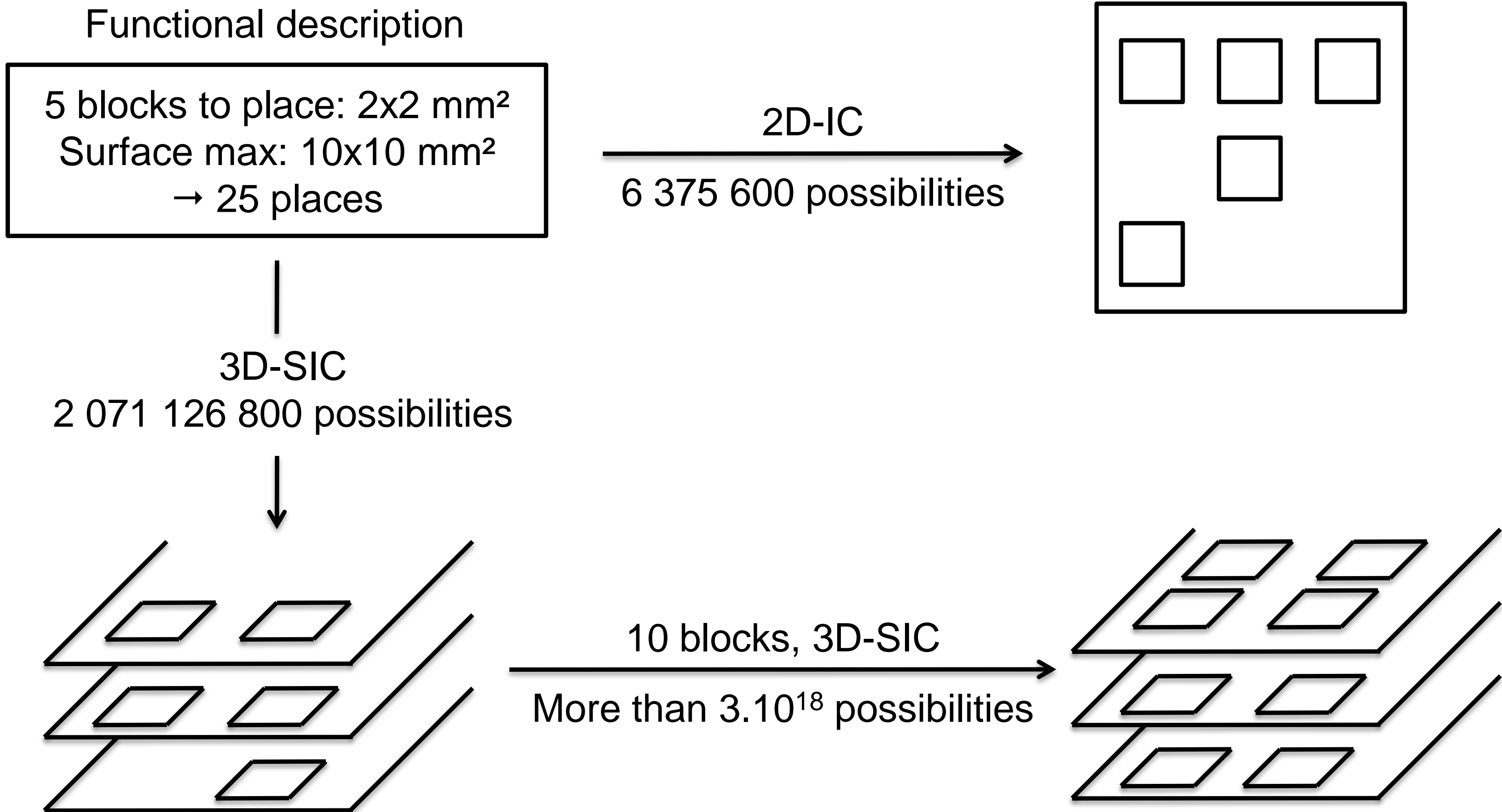


Criteria and design parameters

- Performance
- Consumption
- Cost
- 2D architectural options
- 2D technological options
- Number of tiers
- 3D floorplanning
- 3D architectural options
- 3D technological options

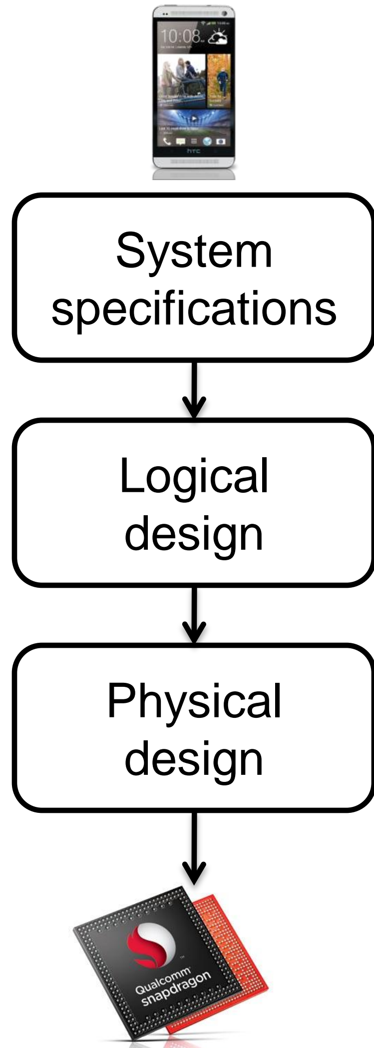
Example of the design space size

ULB



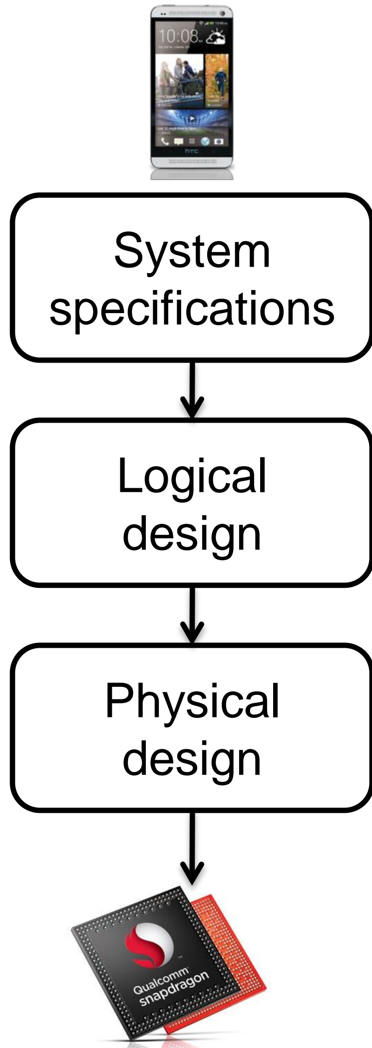
The current design flows are sequential and limit the possible solutions

Classical design flow



The current design flows are sequential and limit the possible solutions

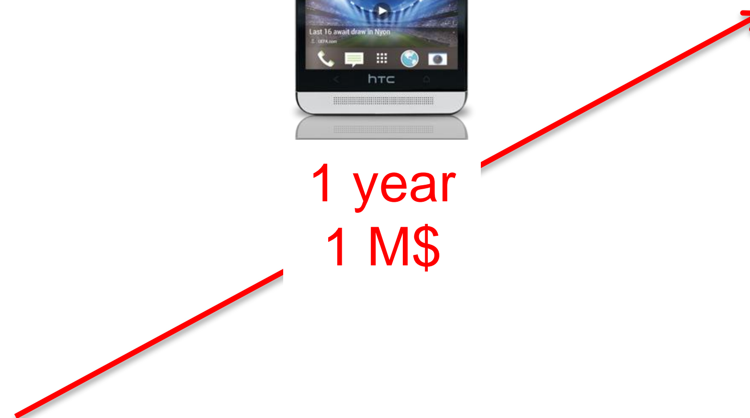
ULB



Disadvantages

- Limitation of the design space exploration
- Local unicriteria optimization at each step
- In practice: several rollbacks, even to the 1st step

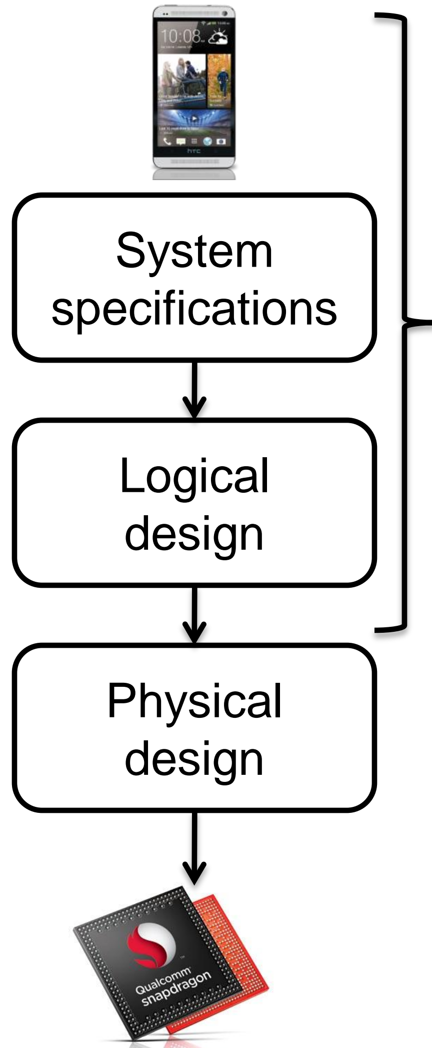
→ Multicriteria optimization not usual



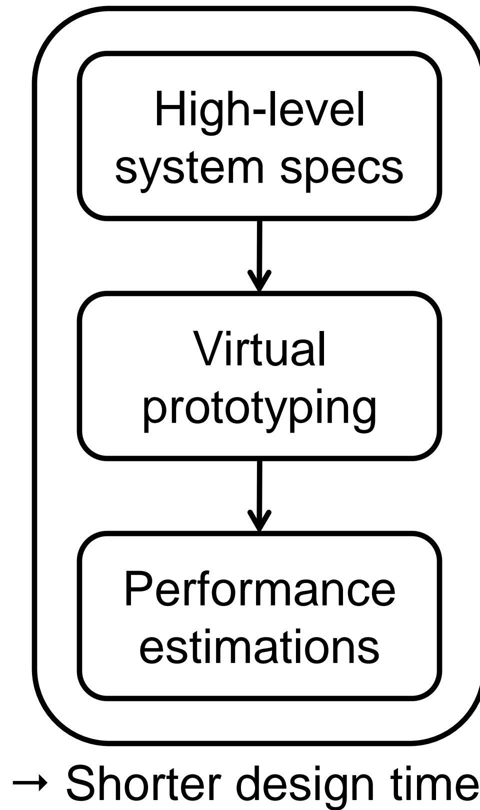
The current improvement is to develop virtual prototyping tools

ULB

Classical design flow

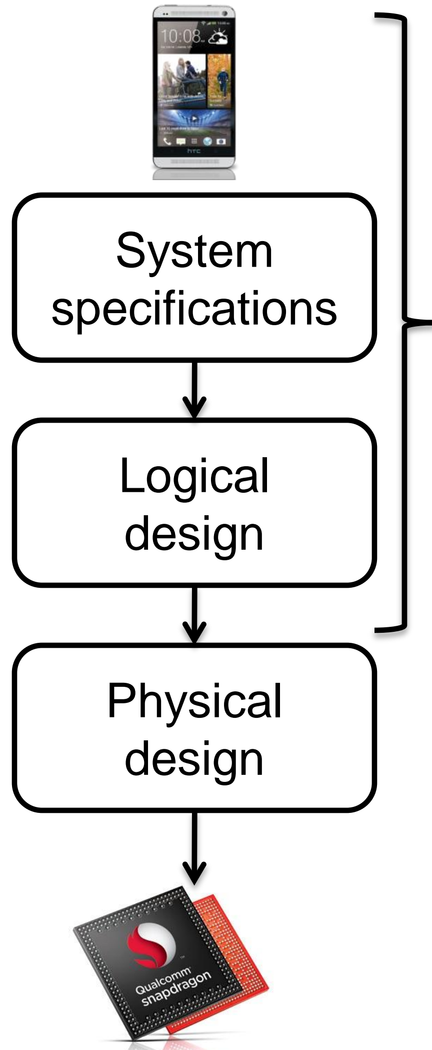


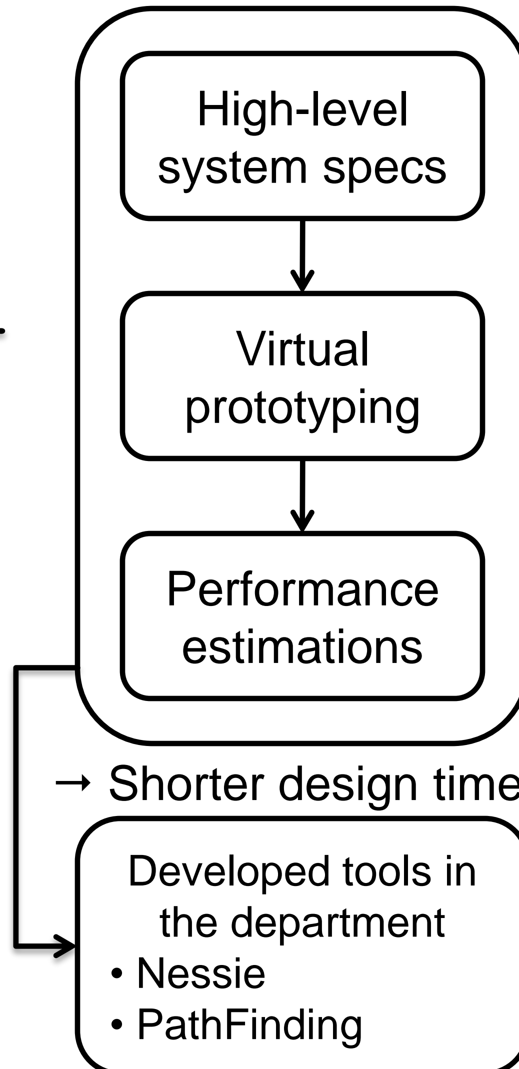
Virtual prototyping flow



→ Shorter design time

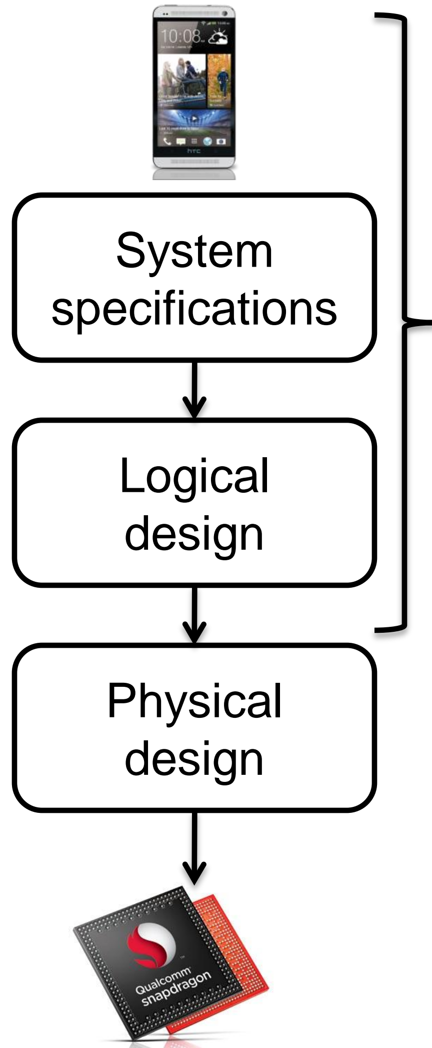
The current improvement is to develop virtual prototyping tools

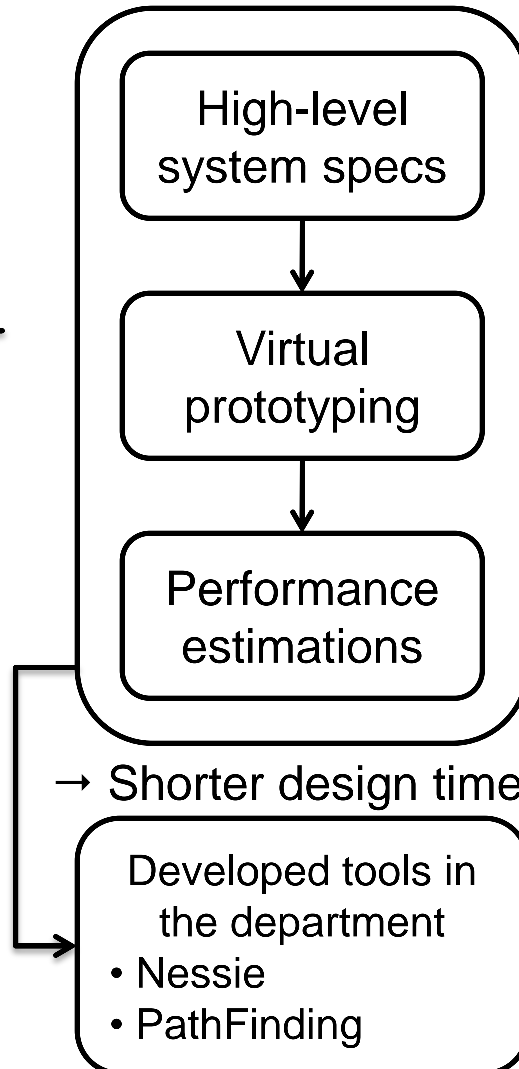




The current improvement is to develop virtual prototyping tools

ULB





Remaining disadvantages

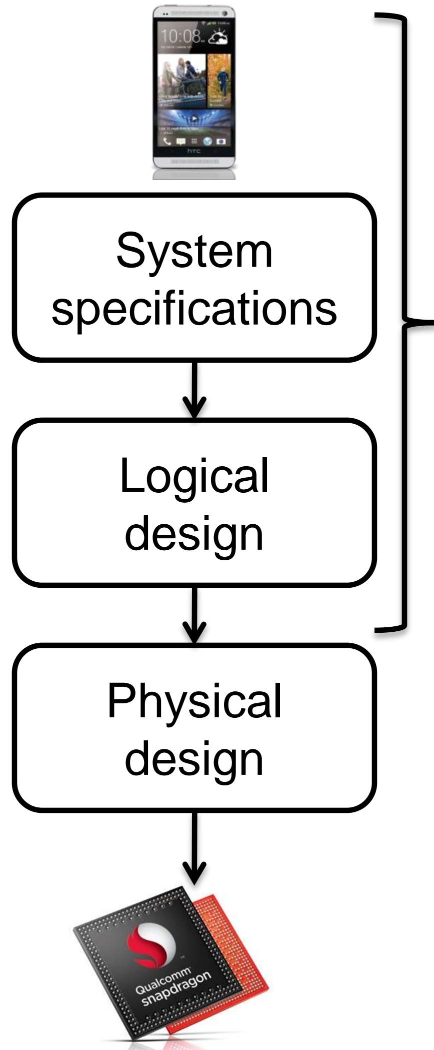
- Limitation of the design space exploration
- Local unicriteria optimization at each step

\+ No 3D-SIC specific tools

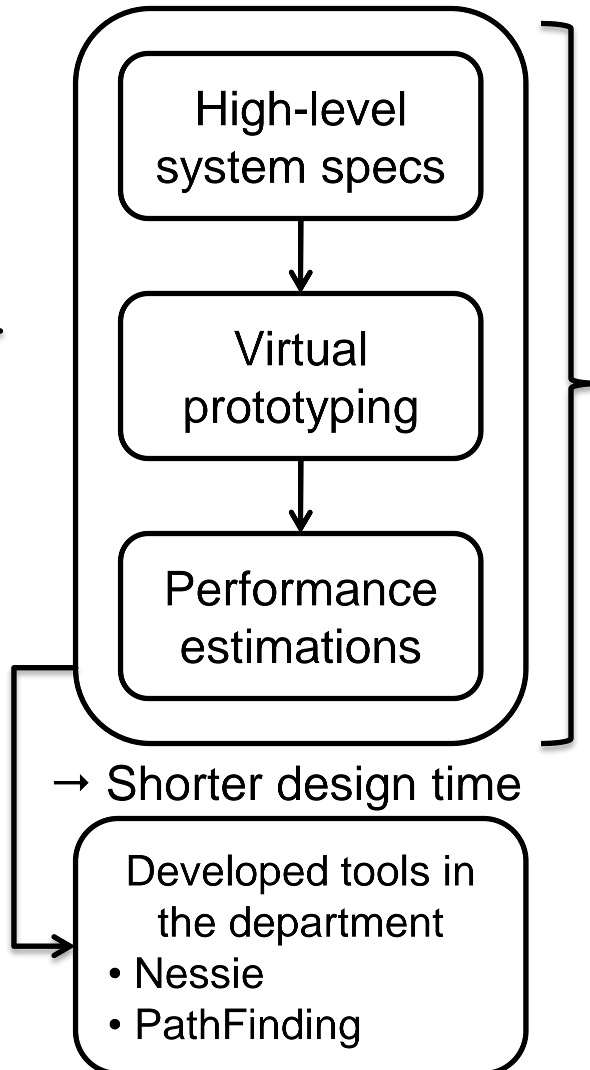
The current improvement is to develop virtual prototyping tools

ULB

Classical design flow



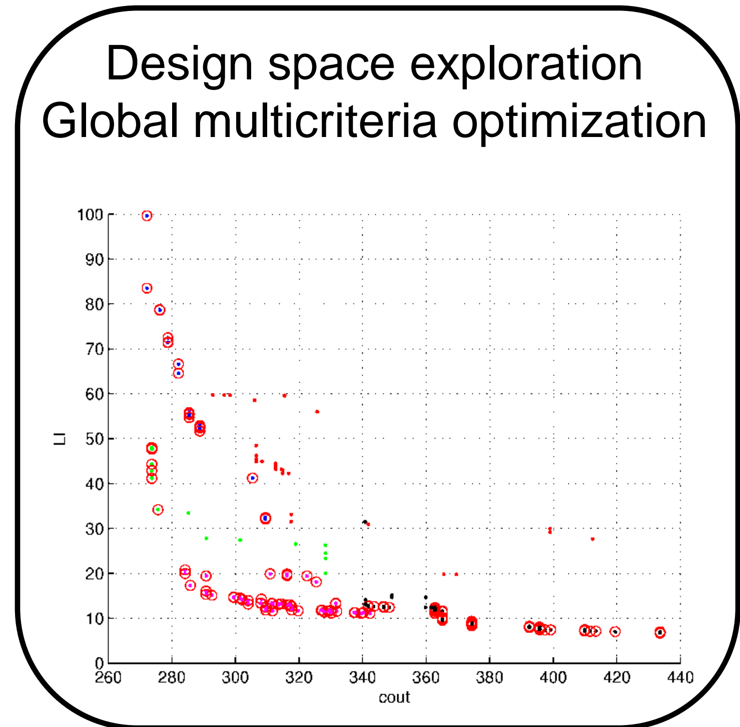
Virtual prototyping flow



→ Shorter design time

Developed tools in the department
- Nessie
- PathFinding

MCDA-based design flow

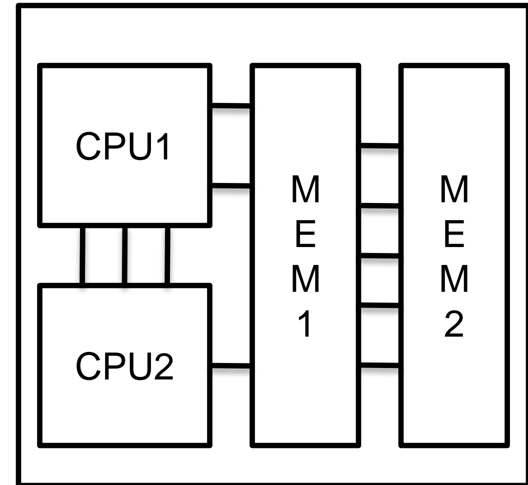


Outline

ULB

- Introduction and current design situation
- Using MCDA
  - Model and criteria
  - Some results
- Conclusion

Modeling an integrated circuit



Outline

ULB

- Introduction and current design situation
- Using MCDA
  - Model and criteria
  - Some results
- Conclusion

Extended degrees of freedom
6 criteria established for the model

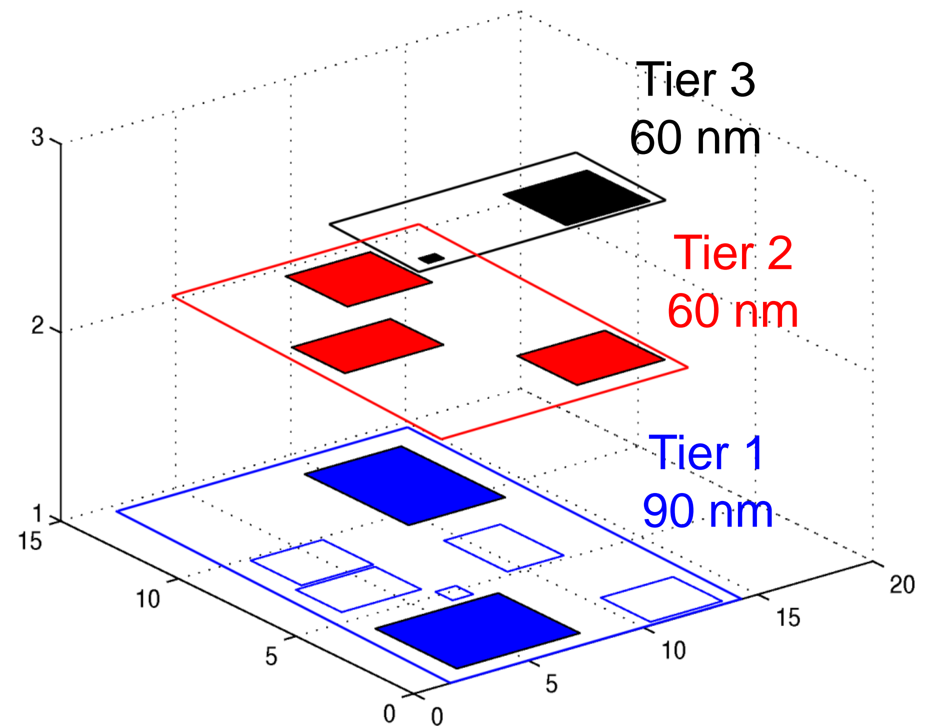
ULB

Degrees of freedom

- Floorplanning: geometrical disposition
- Aspect ratio
- Heterogeneity

Criteria

- Total interconnection length
- Cost
- Packaging volume
- Clock tree position
- Power consumption
- Thermal dissipation

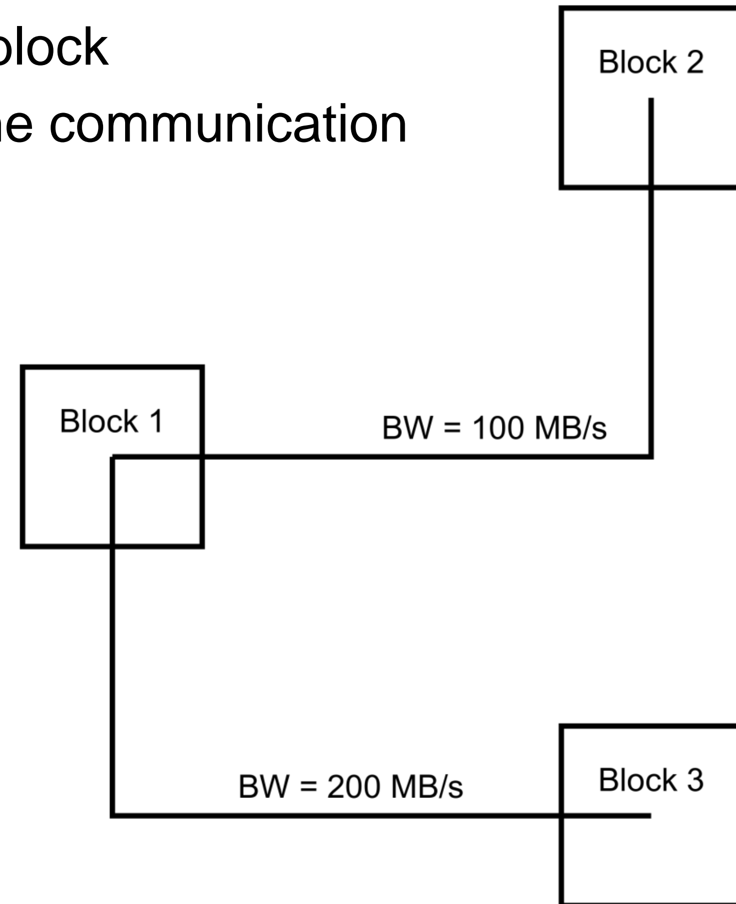


Total interconnection length

ULB

- To minimize
- Computed using the Manhattan distance
- Reference point: center of each block
- Weighted by the bandwidth for the communication

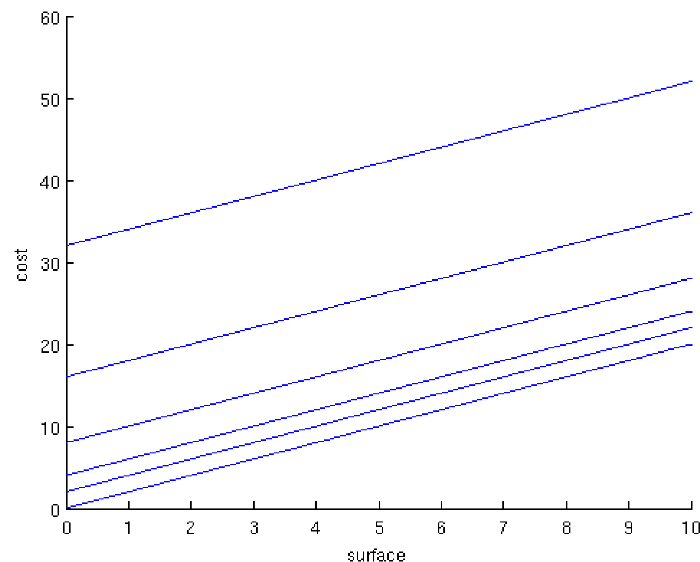
$$\sum_{comm(i,j)} \frac{|x_i - x_j| + |y_i - y_j|}{BW_{ij}}$$



Cost

- To minimize
- Real data are confidential
- Estimation model
  - Proportional to the layers' size
  - Exponential growth with the number of layers
  - Depending on the technology used for manufacturing

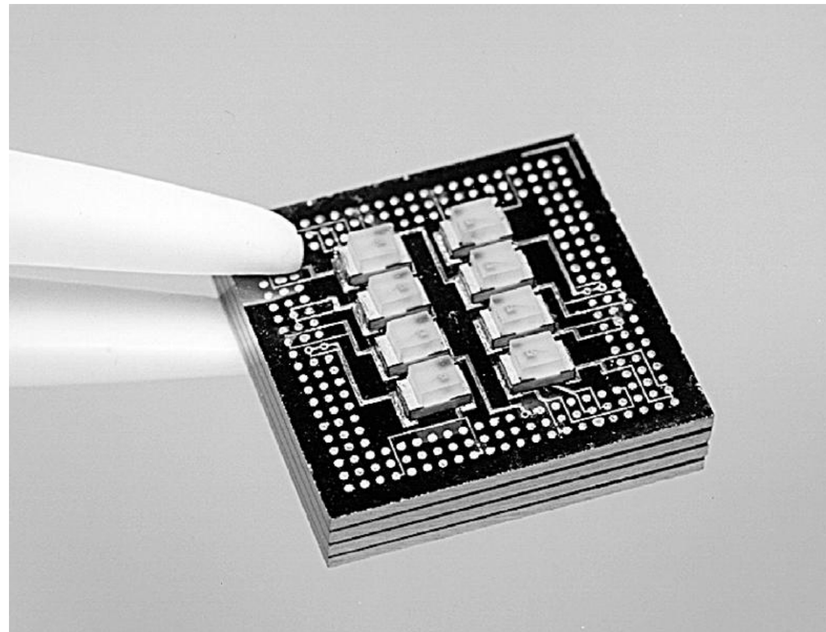
$$cost = a(tech).S + b(tech)^{number\ of\ layers}$$



Packaging volume

ULB

- To minimize
- Critical criterion for embedded systems
- In microelectronics: volume of a parallelepiped

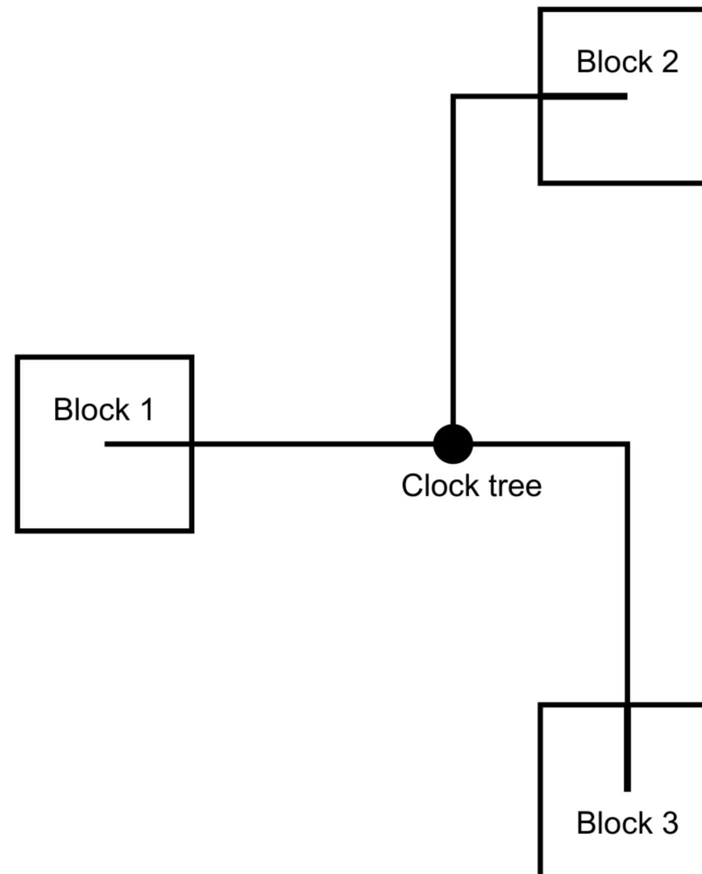


$$volume = \max(S_{layer}) . stack\ thickness$$

Clock tree position

ULB

- Minimizing the distance from the clock tree to all the blocks
- Needed for high working frequency
- Also computed with the Manhattan distance



Power consumption

ULB

- To minimize
- Following electronic laws: sum of static and dynamical consumption

$$P_{tot} = P_{stat} + P_{dyn}$$

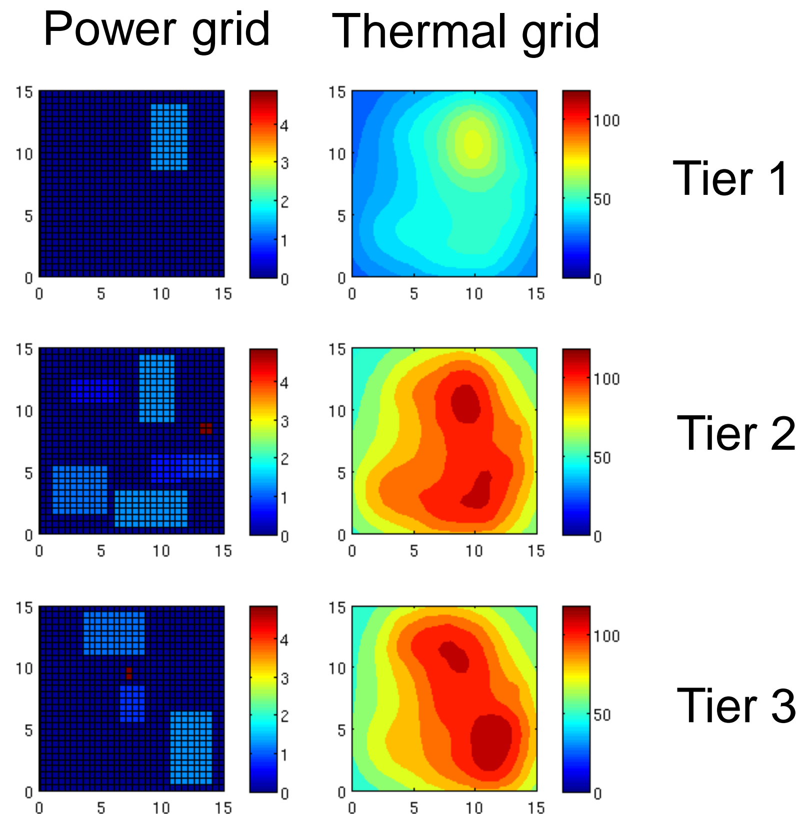
$$P_{stat} = given\ data$$

$$P_{dyn} = \alpha . c_l . l . V^2 . f . [tech]$$

Thermal dissipation

- Must fit constraints
- First simple model with a thermal resistance:

$$P_{diss} = \frac{1}{R_{th,i} . r}$$



Outline

ULB

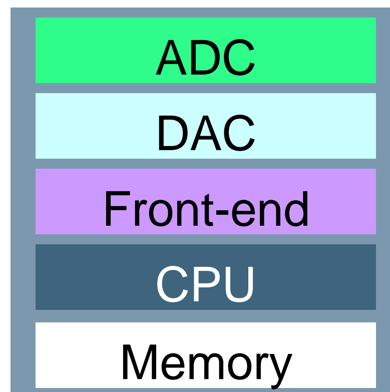
- Introduction and current design situation
- Using MCDA
  - Model and criteria
  - Some results
- Conclusion

Using MCDA tools to design 3D-SIC

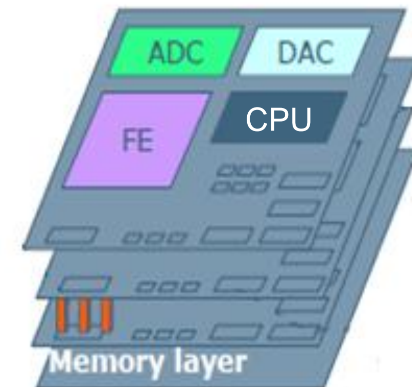
ULB

- Case study: electronic device of 12 blocks,1 to 5 tiers
- Considering 3 criteria: interconnection length (IL), cost and volume
- At first, not considering aspect ratio nor heterogeneity

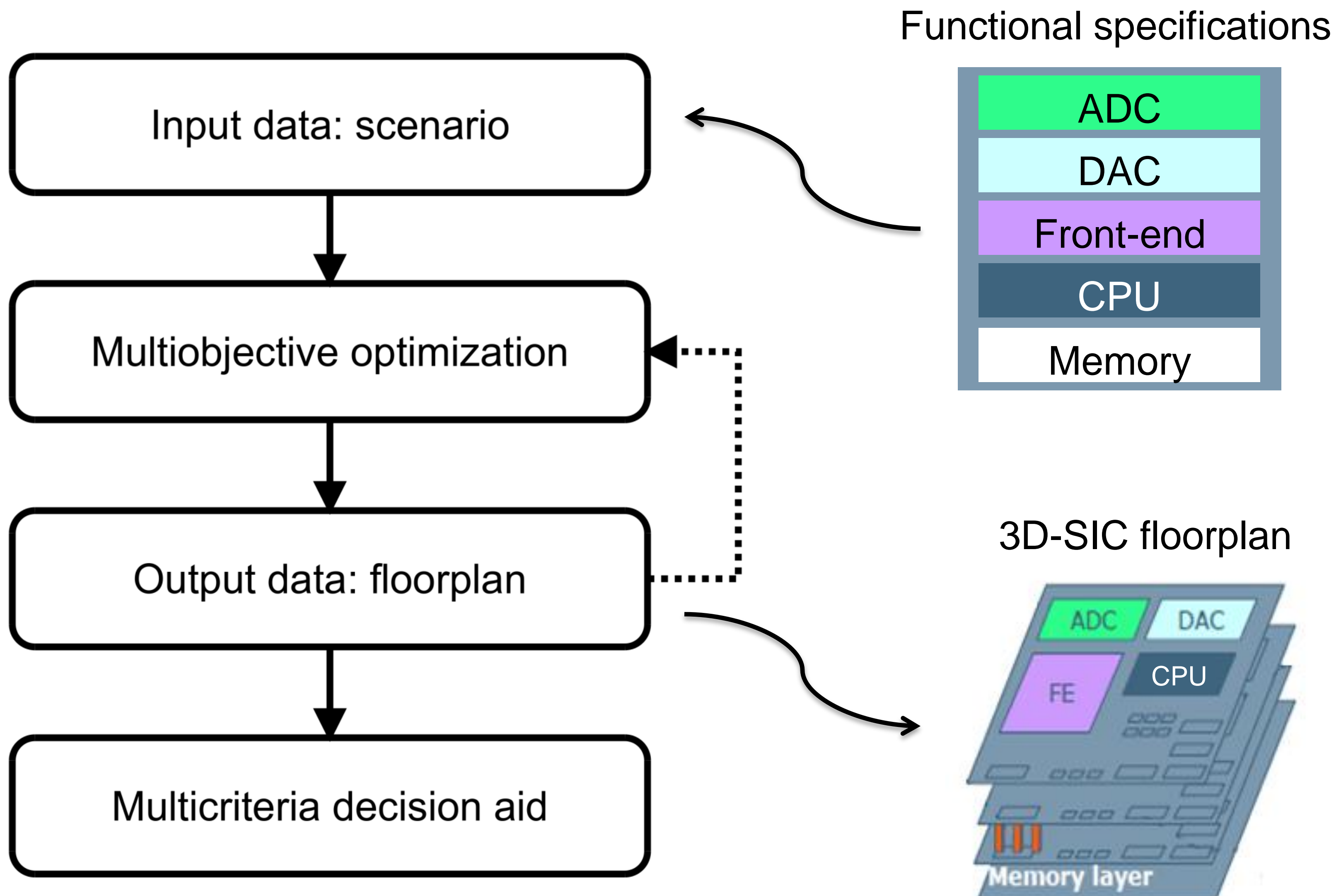
Functional description



How to?

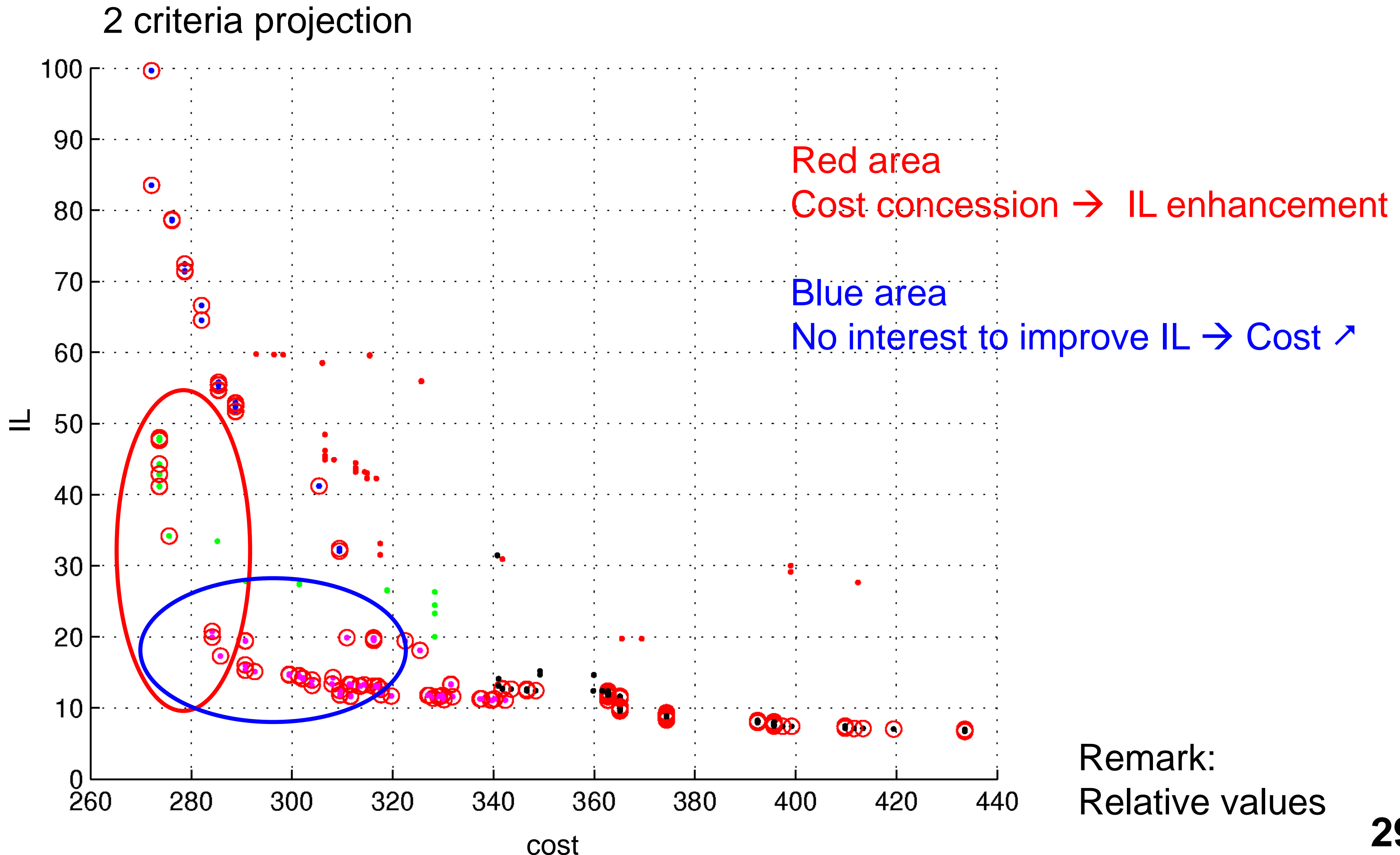


Methodology



MOO & MCDA can give qualitative information that would not be available with current tools

ULB



Remark:
Relative values

MCDA can help in choosing the best compromise alternatives

ULB

- Profile analysis and sorting
- Alternative comparisons
- Compromise choice

zoom=0

delta=95,1%

IL

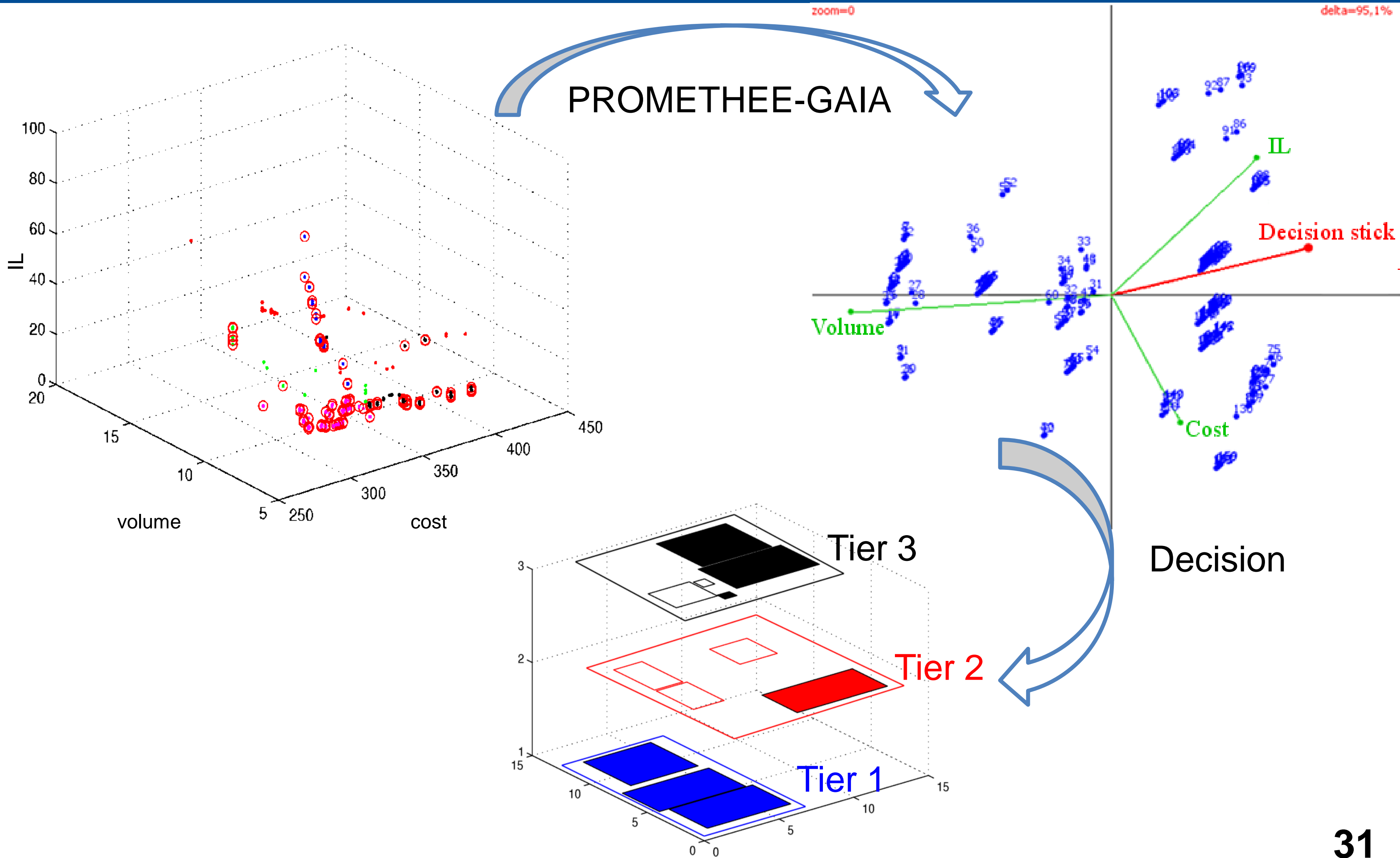
Decision stick

Volume

Cost

Decision aid process

ULB



Outline

ULB

- Introduction and current design situation
- Using MCDA
  - Model and criteria
  - Some results
- Conclusion

Conclusion

ULB

Introduction on using MCDA tools for 3D-SIC design

- 3D-SIC model for multiobjective optimization
- MCDA can give qualitative information that would no be available with current tools
- The flexibility of multiobjective optimization allows more design options than traditional design flows: less restrictions on the design space
- Decision process with PROMETHEE-GAIA

→ Multiobjective optimization and MCDA can support in electronic design

Thank you for your attention!

Any questions?

ECOLE POLYTECHNIQUE DE BRUXELLES

Using the PROMETHEE methodology for the design of 3D-stacked integrated circuits

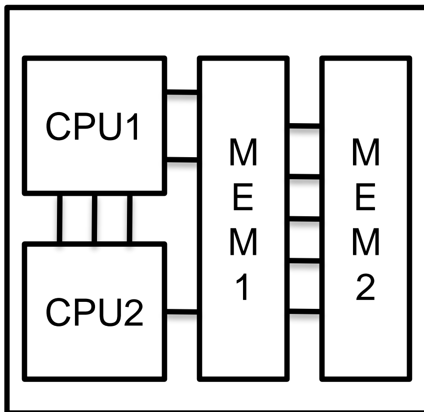
DOAN Nguyen Anh Vu

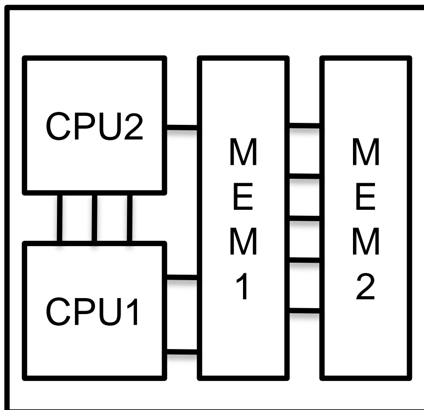
Supervisors: Yves DE SMET
Dragomir MILOJEVIC
Frédéric ROBERT

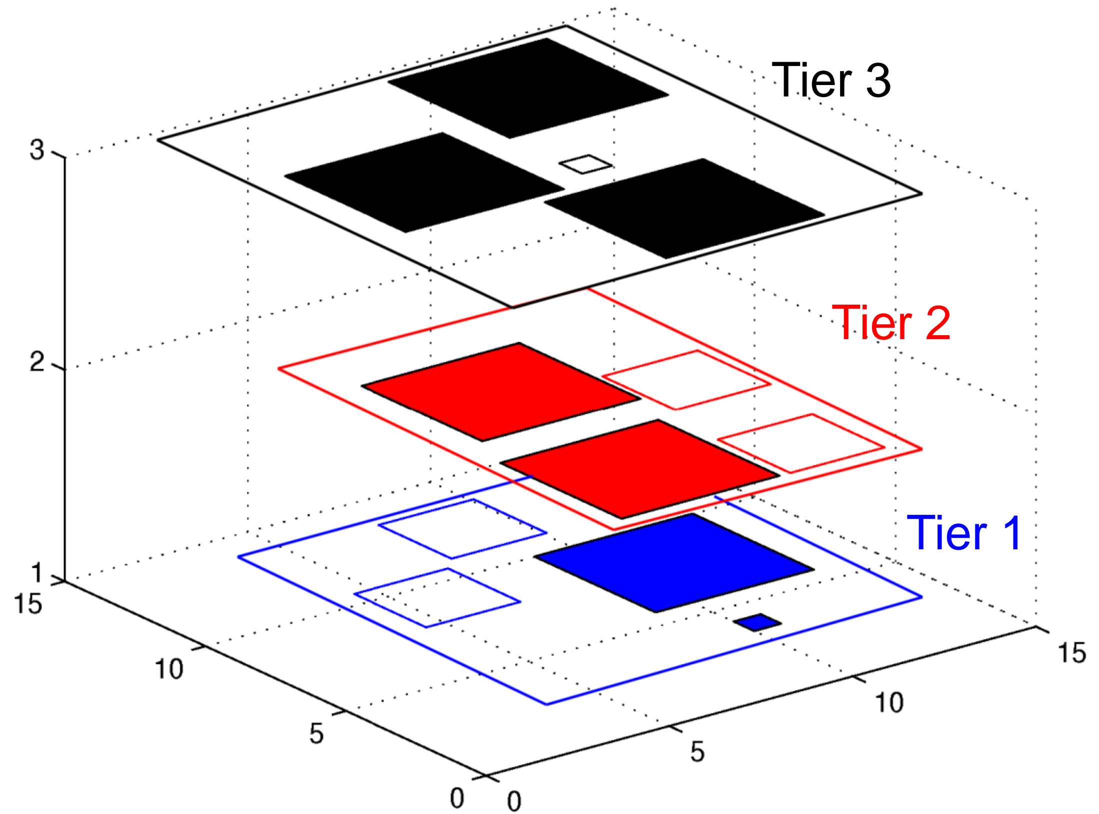
ULB beams

IMW 2014

Degrees of freedom model
Floorplanning: geometrical position of the blocks

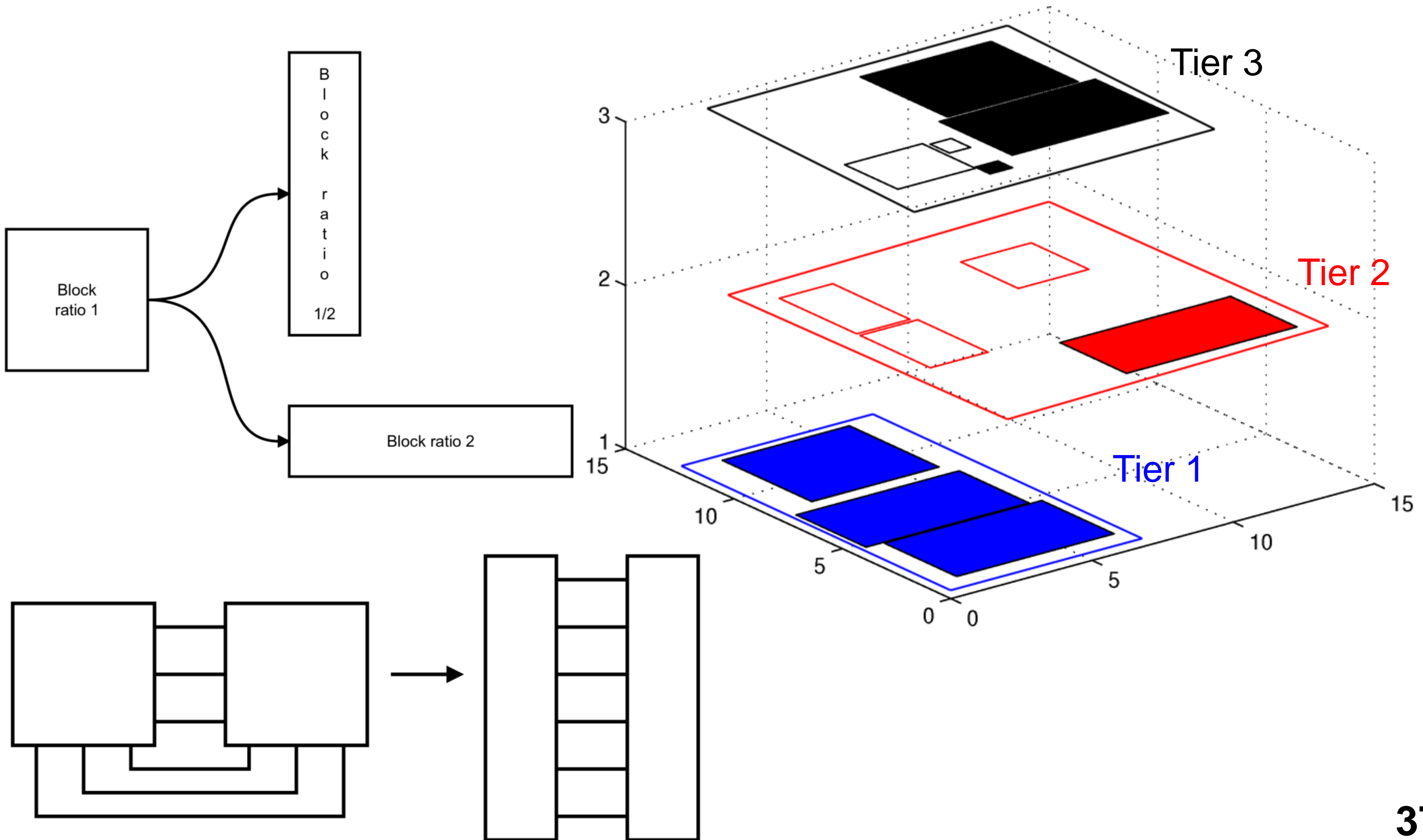






Degrees of freedom model
Aspect ratio of the blocks

ULB



Degrees of freedom
Heterogeneous circuits