Compact Storage Layout based on Custom Hardware to Accelerate Query

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Co-Supervisors: Prof. Torben Bach Pedersen, Prof. Akash Kumar

PERSPECTIVE

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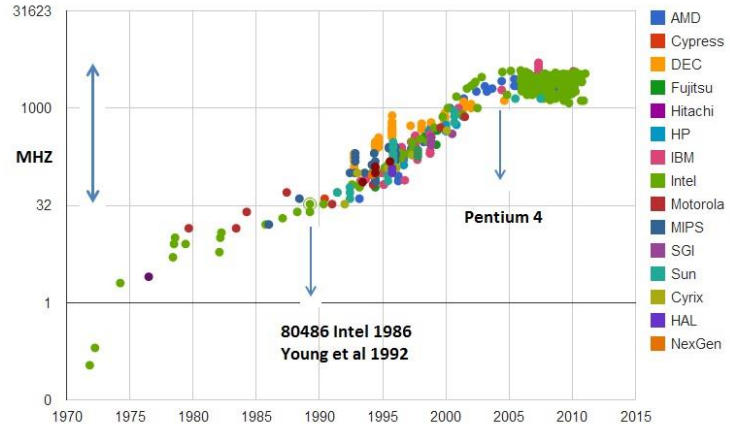

Appears in the Proceedings of the 38th International Symposium on Computer Architecture (ISCA '11)

Dark Silicon and the End of Multicore Scaling

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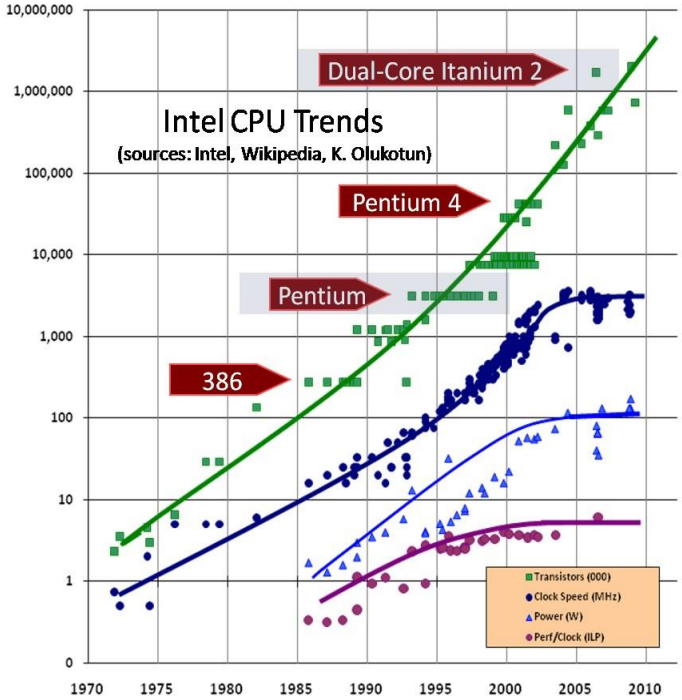
ABSTRACT

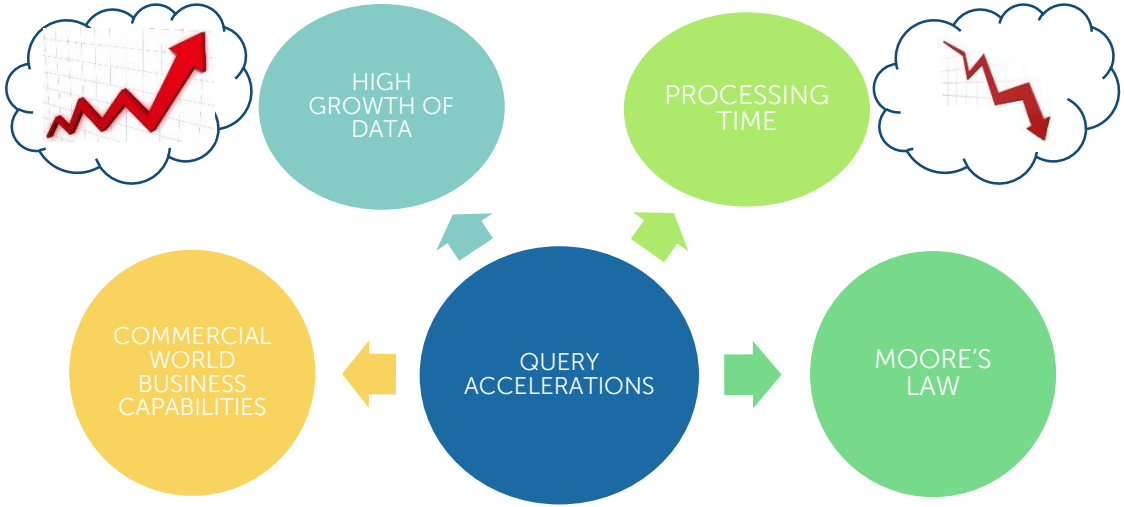
Since 2005, processor designers have increased core counts to exploit Moore's Law scaling, rather than focusing on single-core performance. The failure of Dennard scaling, to which the shift to multicore parts is partially a response, may soon limit multicore scaling just as single-core scaling has been curtailed. This paper models

ture, and compiler advances, Moore's Law, coupled with Dennard scaling [11], has resulted in commensurate exponential performance increases. The recent shift to multicore designs has aimed to increase the number of cores along with transistor count increases, and continue the proportional scaling of performance. As a result, architecture researchers have started focusing on 100-core and 1000-core chips and related research topics and called for changes



http://www.extremetech.com/wp-content/uploads/2012/02/CPU-Scaling.jpg

MOTIVATION


HIGH GROWTH OF DATA
PROCESSING TIME
COMMERCIAL WORLD BUSINESS CAPABILITIES
QUERY ACCELERATIONS
MOORE'S LAW


DATA


Data Processing

Hardware Trends

CPUs
- Sequential Processing
- Implementation on Software
- Execution non deterministic

CPU

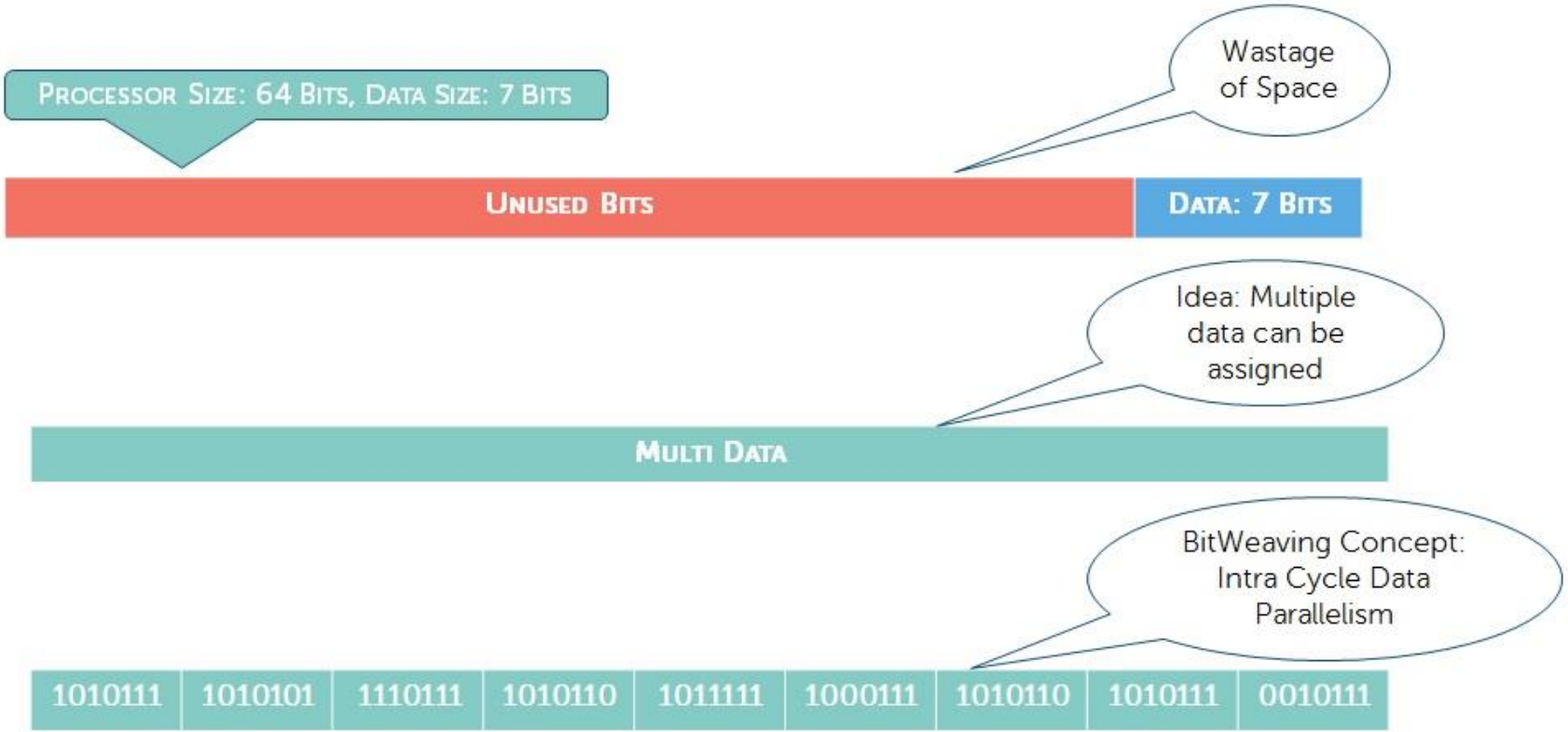
GPUs
- Limited Parallel Processing
- Implementation on Software
- Execution fast

GPU

FPGAs
- Massive Parallel Processing
- Implementation on Hardware
- Extremely fast execution

FPGA

Storage Layouts



STORAGE LAYOUTS- BITWEAVING

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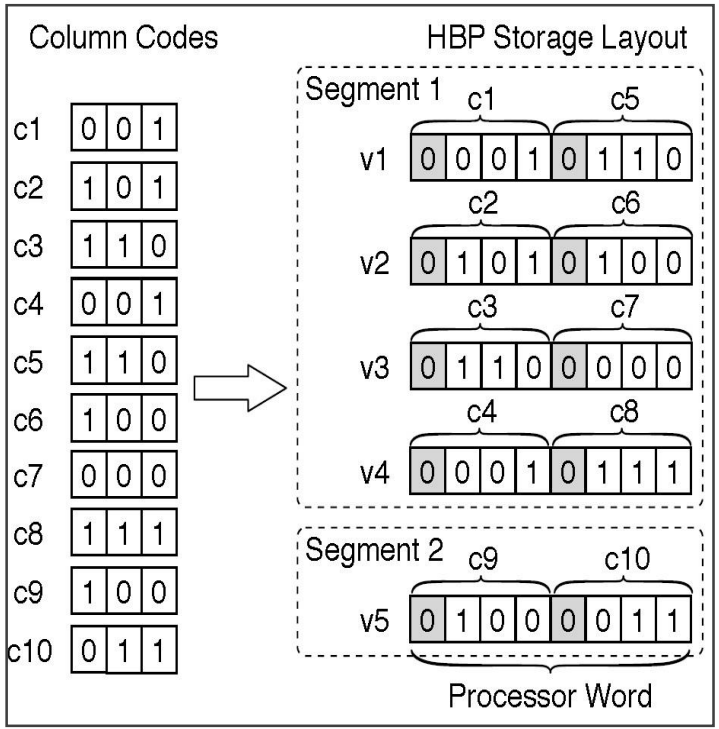
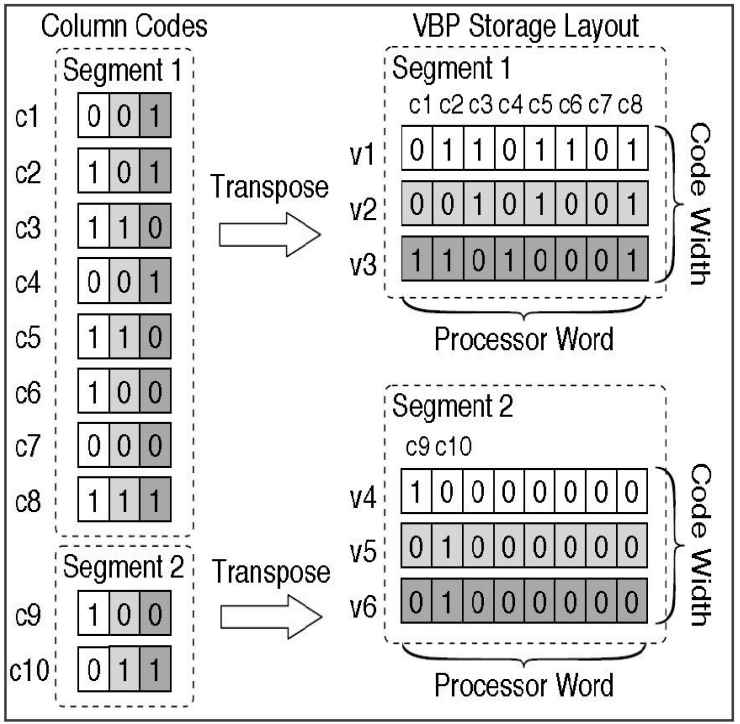
Horizontal



Vertical



Ref: Yinan Li and Jignesh M. Patel, BitWeaving: fast scans for main memory data processing. Proceedings of the ACM SIGMOD International Conference on Management of Data 2013, NY, USA, pp.289-300.

HORIZONTAL BITWEAVING (INSTRUCTION EVALUATION)

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$3 < C_i$?

COLUMN CODES

C_1	0	0	1
C_2	0	1	1
C_3	1	1	0
C_4	1	0	0
C_5	0	0	1
C_6	1	0	0
C_7	1	1	0
C_8	1	1	0

H_1	0	0	0	1	0	0	1	1
H_2	0	1	1	0	0	1	0	0
H_3	0	0	0	1	0	1	0	0
H_4	0	1	1	0	0	1	1	0

Horizontal BitWeaving Layouts of the given column codes

Q_1	0	0	1	1	0	0	1	1

Horizontal BitWeaving Layout of 3

Horizontal BitWeaving layout of Inverse 3

Q'_1	0	1	0	0	0	1	0	0

HORIZONTAL BITWEAVING (INSTRUCTION EVALUATION)

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H_1	0	0	0	1	0	0	1	1
Q'_1	0	1	0	0	0	1	0	0
S_1	0	1	0	1	0	1	1	1

H_2	0	1	1	0	0	1	0	0
Q'_1	0	1	0	0	0	1	0	0
S_2	1	0	1	0	1	0	0	0

H_3	0	0	0	1	0	1	0	0
Q'_1	0	1	0	0	0	1	0	0
S_3	0	1	0	1	1	0	0	0

H_4	0	1	1	0	0	1	1	0
Q'_1	0	1	0	0	0	1	0	0
S_4	1	0	1	0	1	0	1	0

PIPELINE CUSTOM HARDWARE (HORIZONTAL BITWEAVING)

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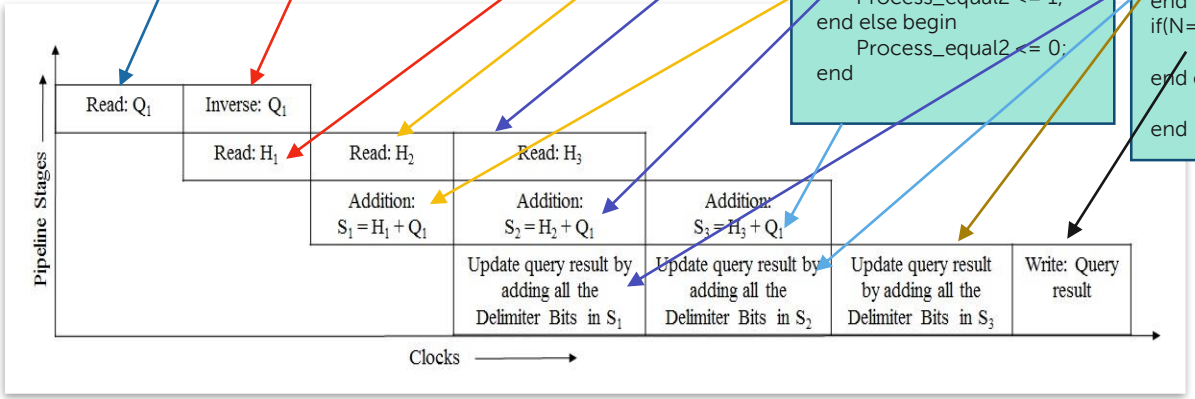
```
2'b01: begin
        if(S_AXIS_TVALID == 1)begin
            Q <= S_AXIS_TDATA;
            state1<= 2;
            Read_Input <= 1;
         end else
            state1<= 1;
       end
```

```
if(Read_Input == 1 && S_AXIS_TVALID == 1
&& state1==2)begin
        H  <= S_AXIS_TDATA;
        Process_equal1 <= 1;
end else begin
       Process_equal1 <= 0;
end
```

```
Q <= Q ^ 32'hffffffff;
```

```
if(Process_equal1 == 1)begin
        S <= H + Q;
        Process_equal2 <= 1;
end else begin
       Process_equal2 <= 0;
end
```

```
if(Process_equal2 == 1)begin
     sum <= sum + S[31]+S[27]+S[23]+S[19]+S[15]+S[11]+S[7]+S[3];
      N1 <= N1+1;
end
if(N==N1 && N!=0)begin
      Write_Output <= 1;
end else begin
       Write_Output <= 0;
end
```



VERTICAL BITWEAVING (INSTRUCTION EVALUATION)

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COLUMN CODES

$3 = C_i$?

1
3
6
4
1
4
6
6

0	0	1	1	0	1	1	1	V_1
0	1	1	0	0	0	1	1	V_2
1	1	0	0	1	0	0	0	V_3

Vertical BitWeaving Layouts of the given column codes

0	0	0	0	0	0	0	0	Q_1
1	1	1	1	1	1	1	1	Q_2
1	1	1	1	1	1	1	1	Q_3

Vertical BitWeaving Layout of 3

VERTICAL BITWEAVING (INSTRUCTION EVALUATION)

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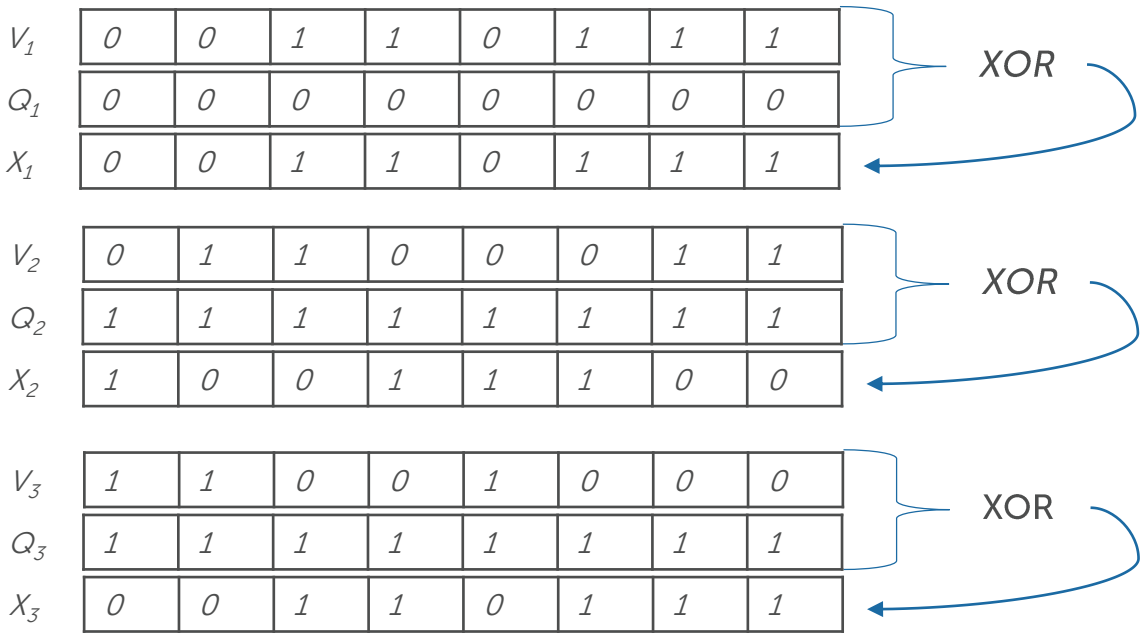
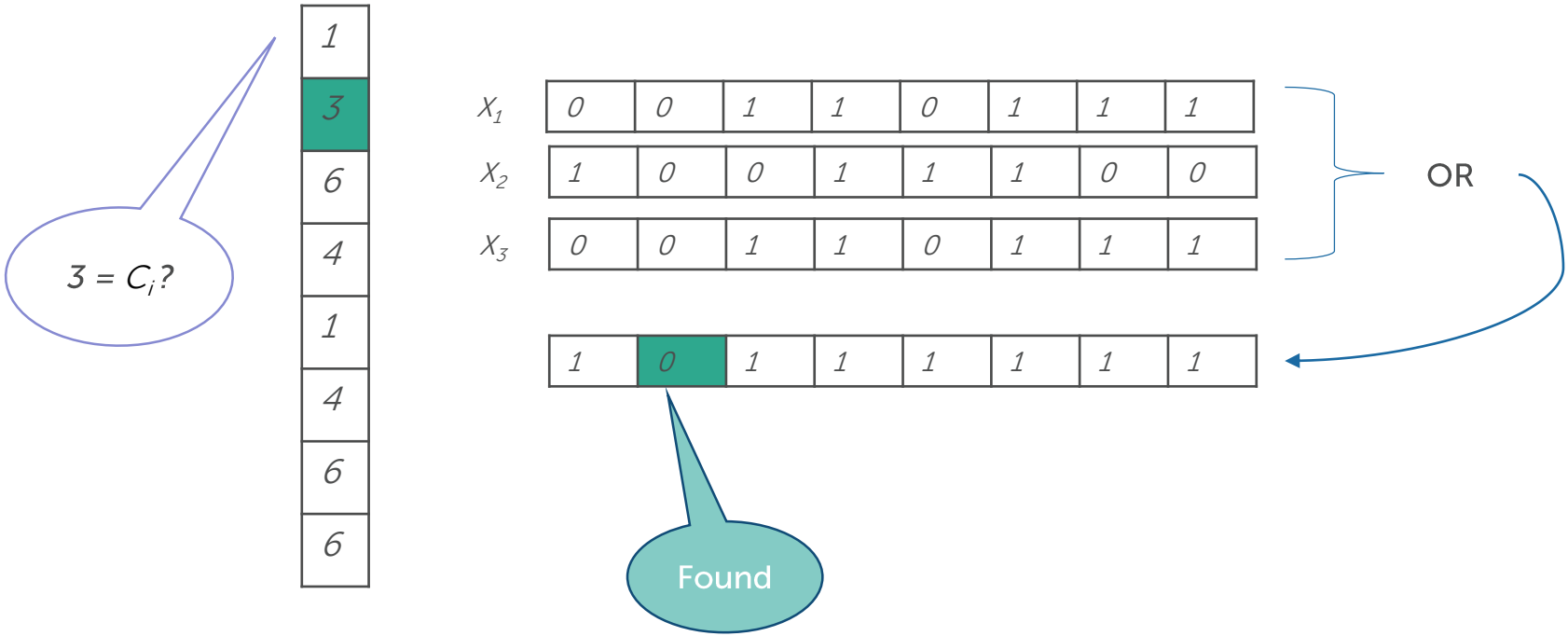


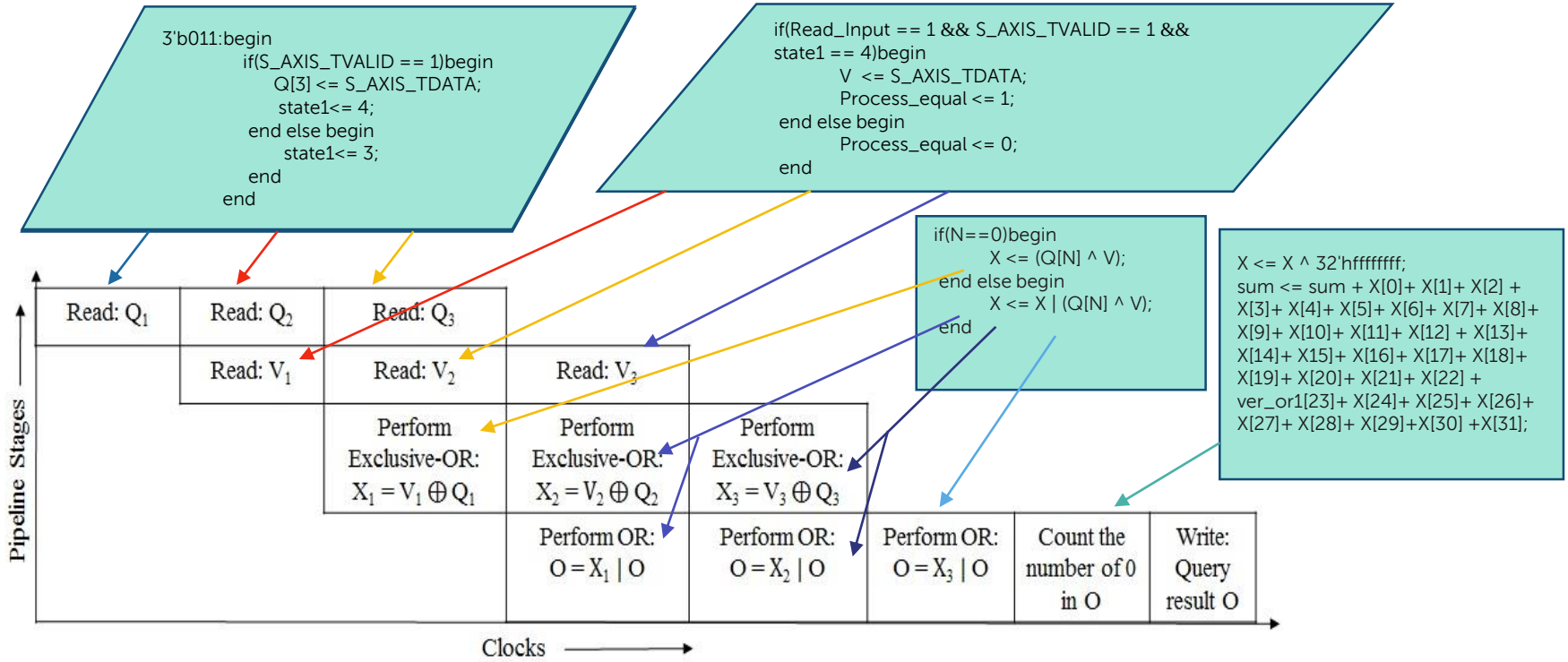
VERTICAL BITWEAVING (INSTRUCTION EVALUATION)

Dresden Database Systems Group



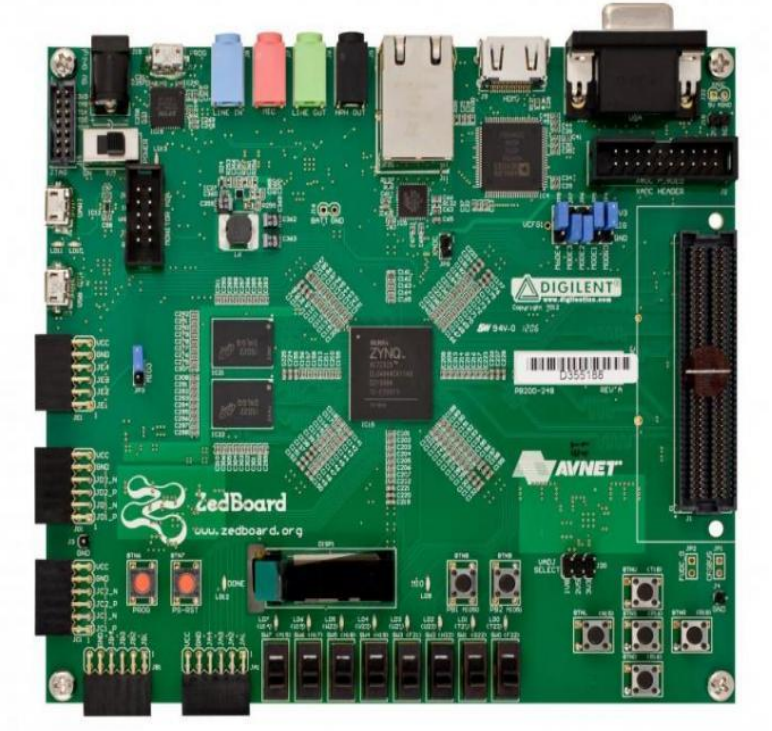
PIPELINE CUSTOM HARDWARE (VERTICAL BITWEAVING)

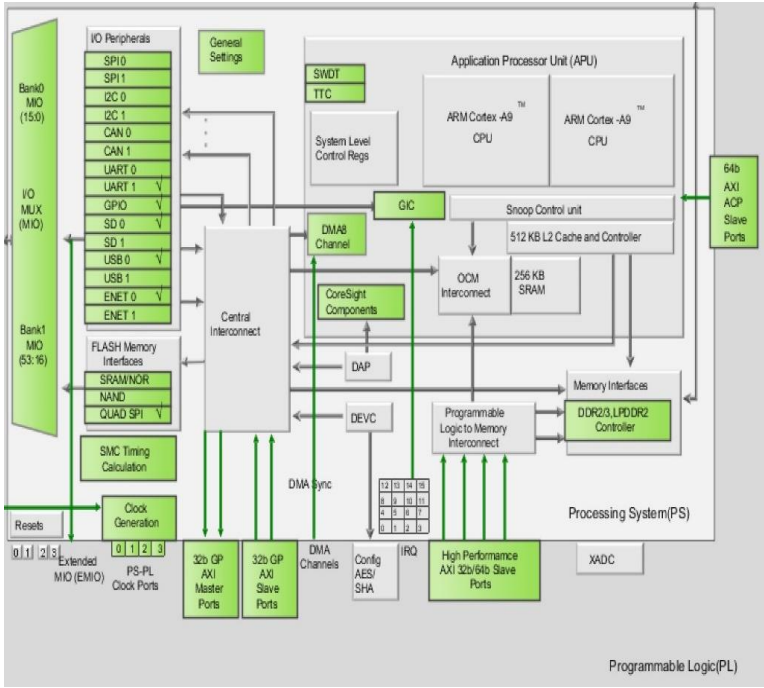
Dresden Database Systems Group



Zynq ZedBoard

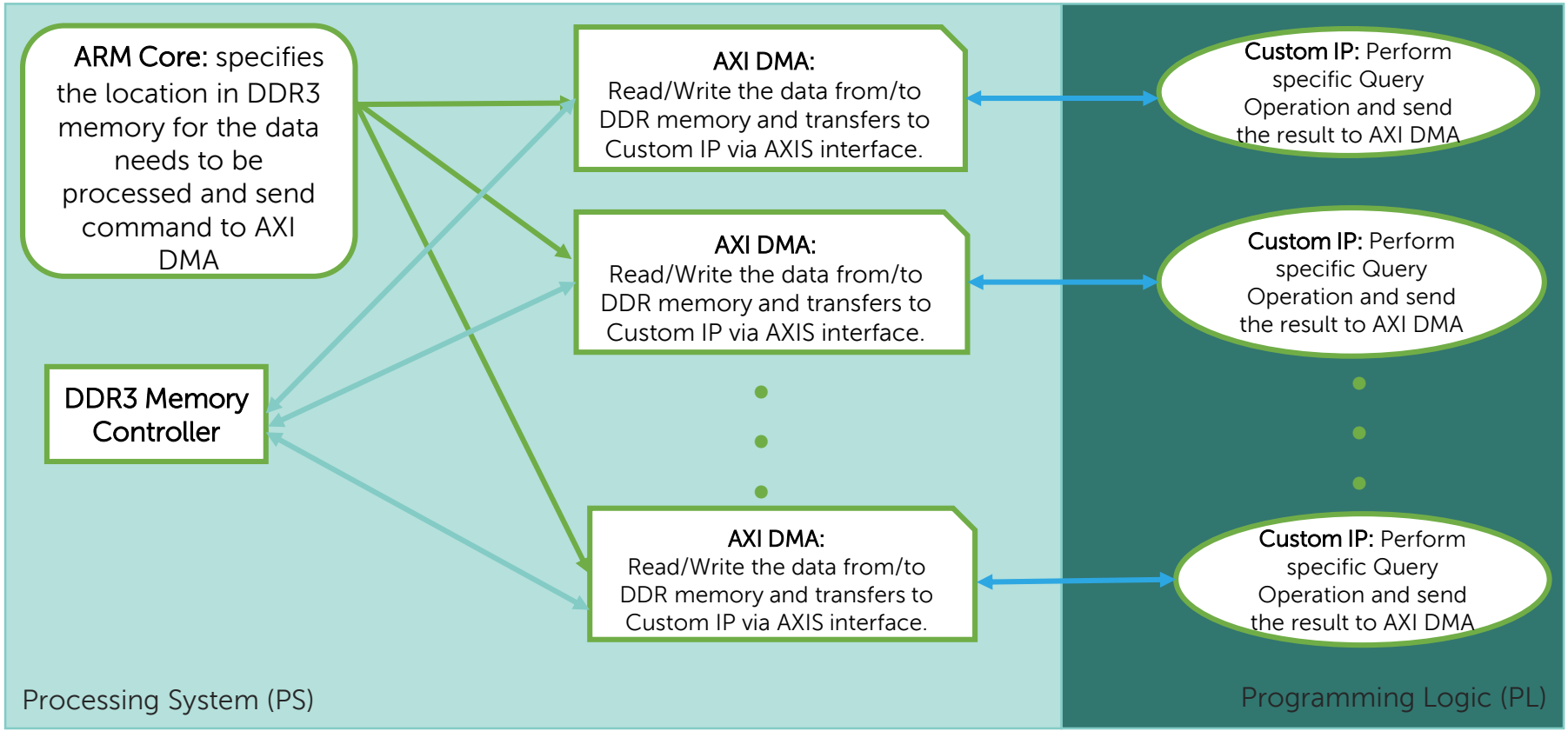
Dresden Database Systems Group





Zynq ZedBoard: Hardware Design

Dresden Database Systems Group



Multiple Custom IPs Performance (Linear Layout) on Zynq ZedBoard

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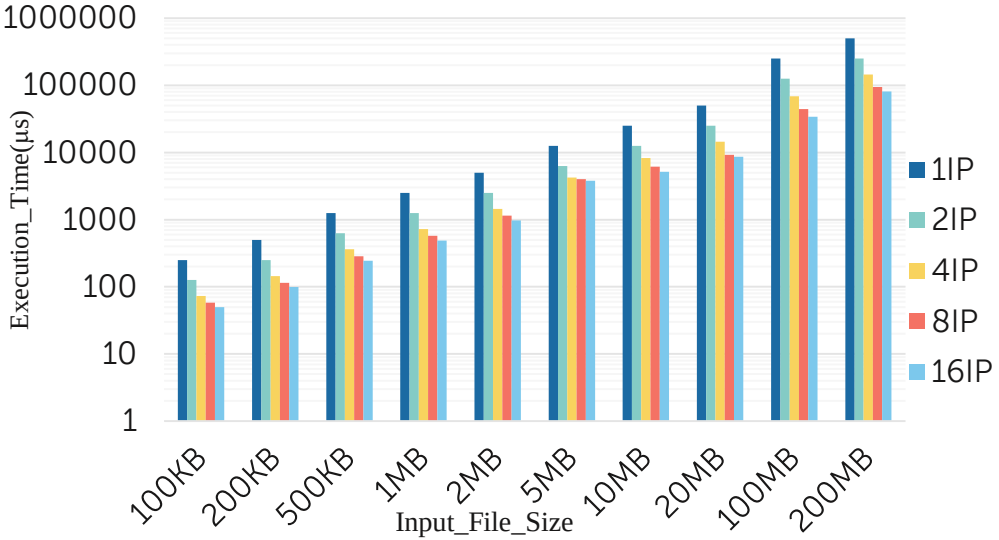
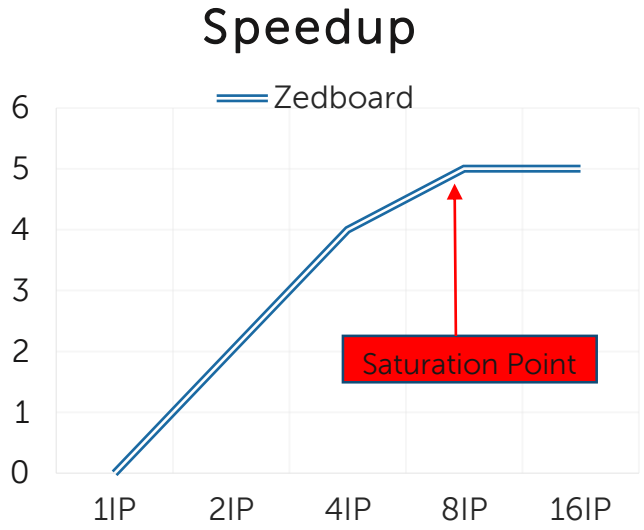
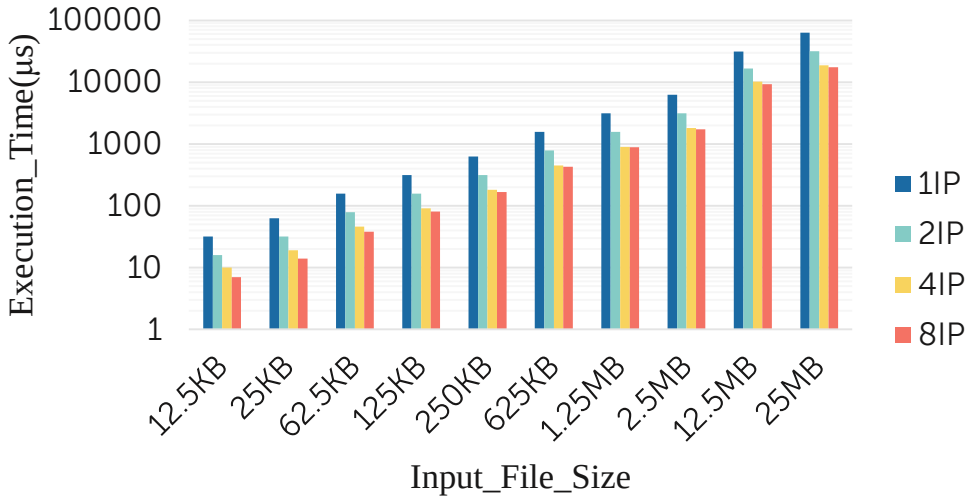
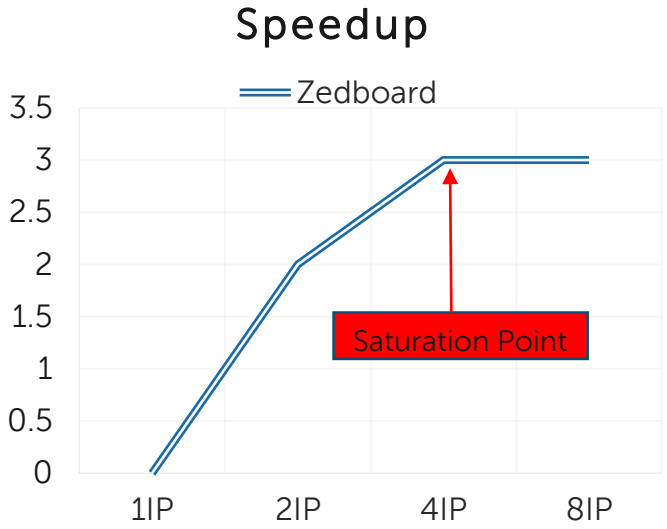




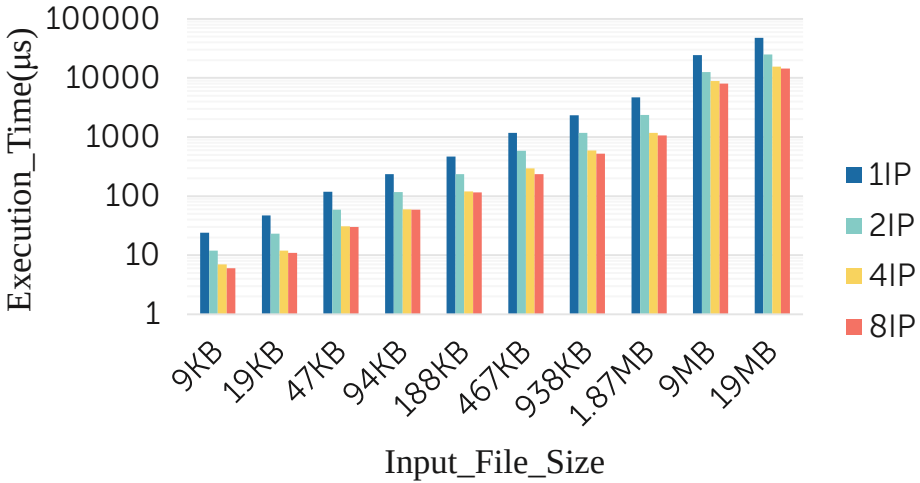
Multiple Custom IPs Performance (Horizontal Layout) on Zynq ZedBoard

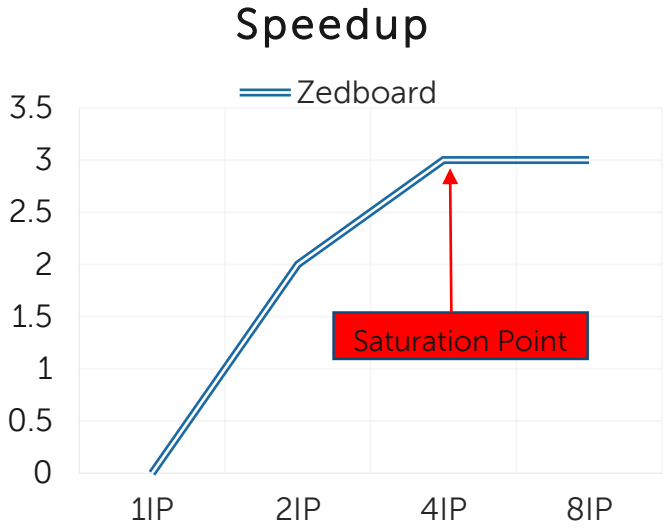




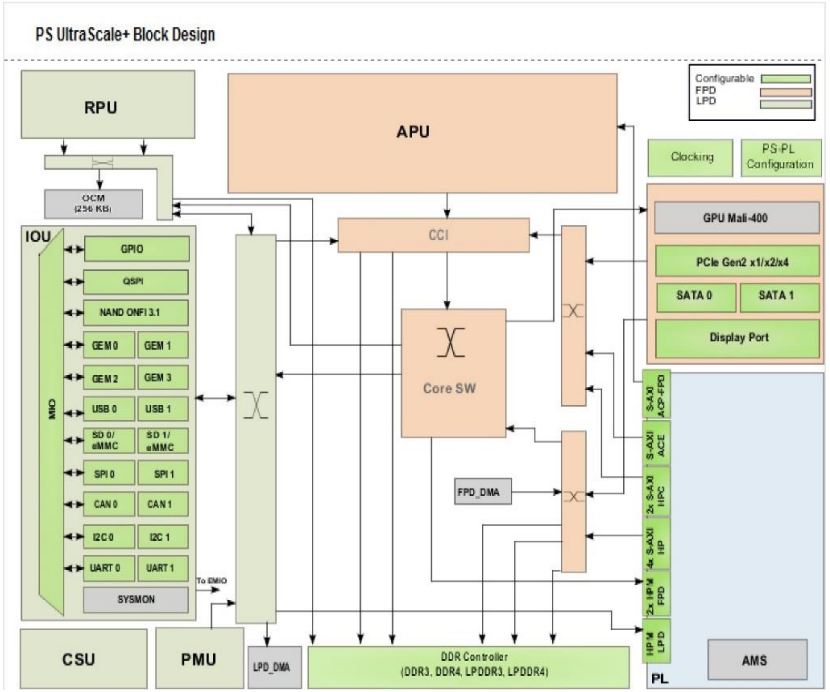
Multiple Custom IPs Performance (Vertical Layout) on Zynq ZedBoard

Dresden Database Systems Group



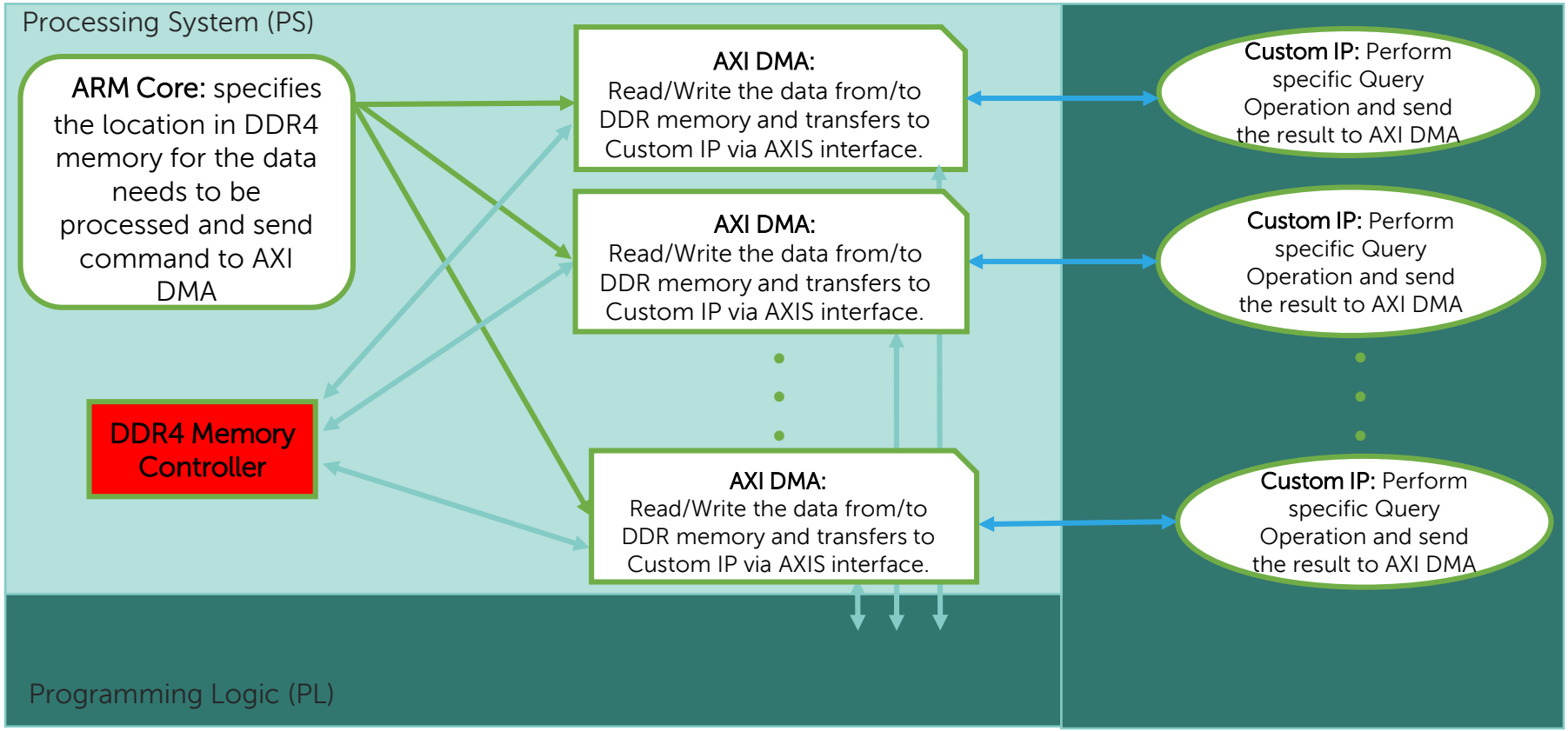


Zynq Ultrascale+

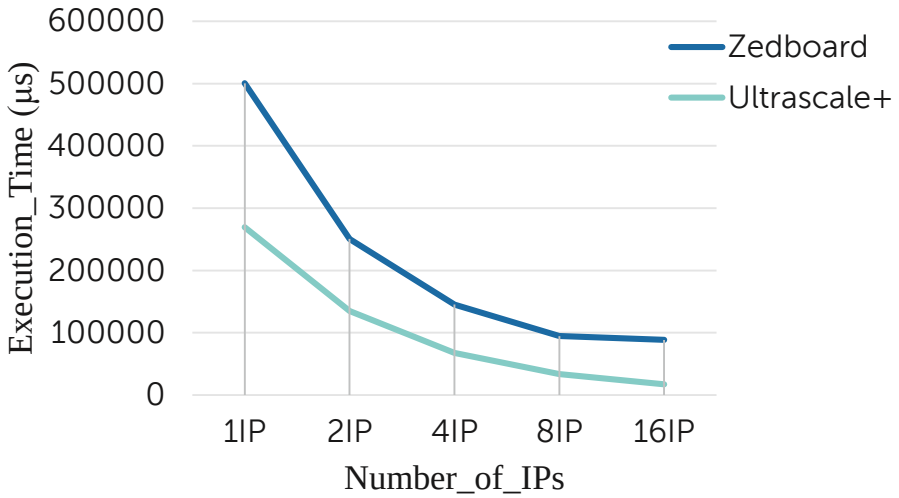


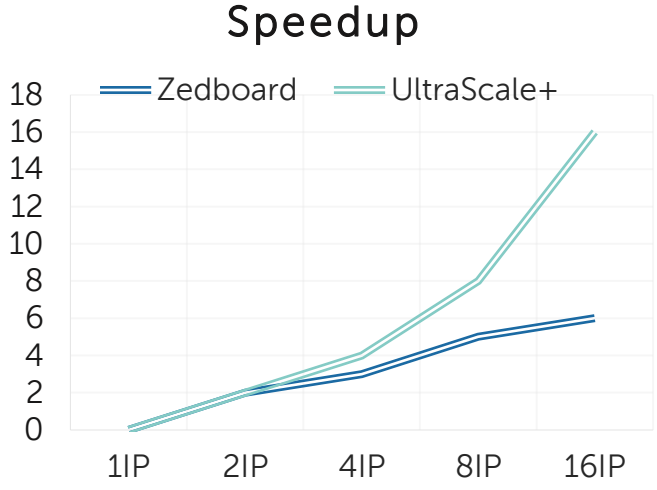
Zynq Ultrascale+: Hardware Design

Dresden Database Systems Group

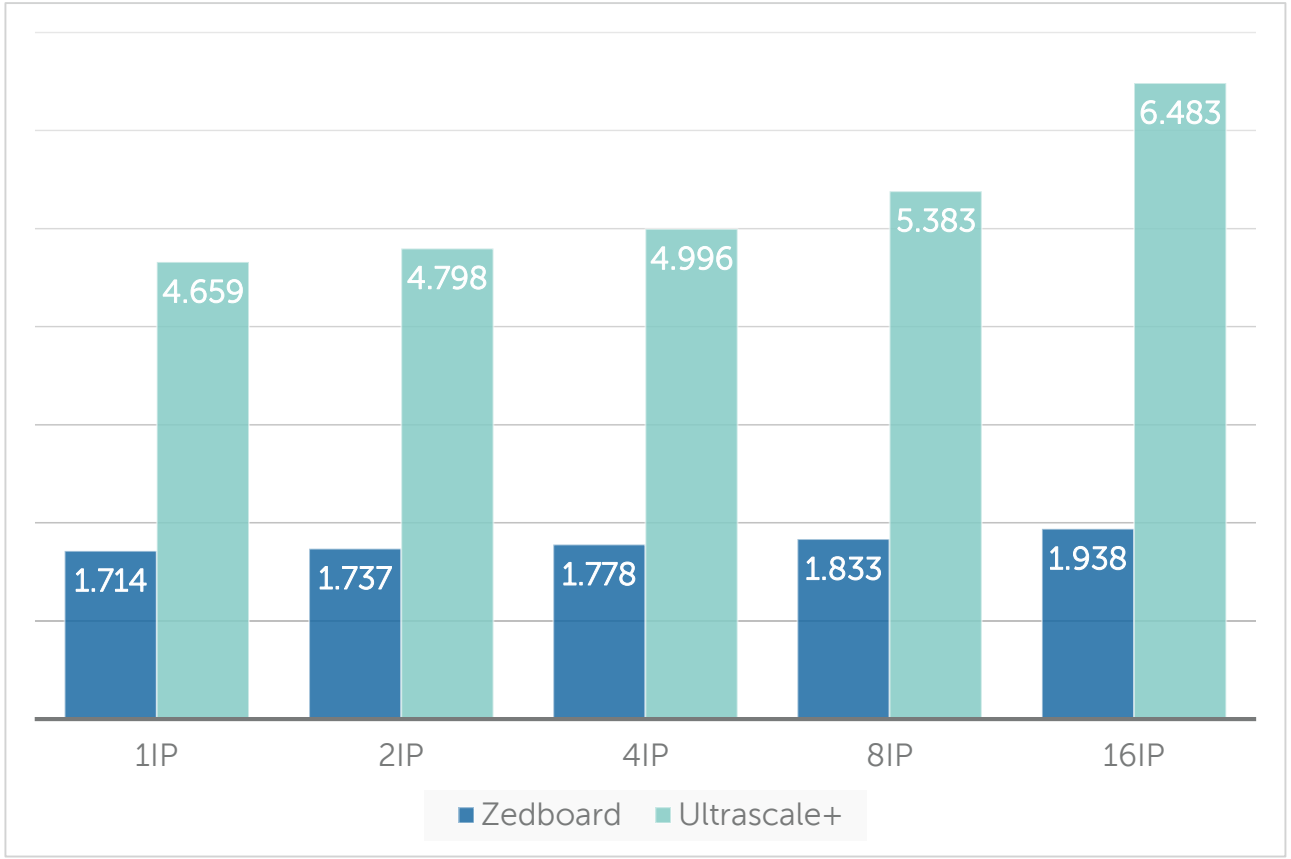


Zynq Zedboard vs. Zynq Ultrascale+





Zynq Zedboard vs. Zynq Ultrascale+ (Power)



Submitted Paper and Future Works

Dresden Database Systems Group

- "Demystifying FPGAs"
  - Venue : ADMS 2017.
  - Demystifying FPGAs parallelism characteristics using custom hardware for query acceleration.
  - This paper gives an overview of FPGAs parallelism behavior to accelerate query by running replicate custom hardware in parallel and investigate the reason of get saturate at a certain level.

Taking break from It4bi-DC for Cfaed Orchestration Path at TUD for one year.

- Working on scalability of compact storage layouts based hardware designs on Zynq Ultrascale+ Board.
- Thinking about new compact storage layout.
- Thinking about high level query operations.

Thank You

Courses

Dresden Database Systems Group

Activity	Place/Organised by	ECTS	General/Project course	Status
Foreign Language (German)	TUD	2.5	General	Completed, Winter 2016/2017
Transactional Information System	TUD	6	General	Completed, Winter 2016/2017
Big Data Management on Modern Hardware	AAU	2	General	Completed, Winter 2016/2017
Writing and Reviewing of Scientific Papers	TUD/AAU	1	General	Planned, Summer 2017
Foreign Language (Danish)	AAU	2.5	General	Planned, Winter 2018/2019
Introduction to the Phd Study	AAU	1	General	Planned, Winter 2018/2019
Aspects of Advanced Analytics	AAU	2	General	Planned, Summer 2018
EBISS Summer School	IT4BI	2	Project	Planned
IT4BI-DC Doctoral Colloquium	IT4BI	3	Project	Planned
Conference Attendance	TBD	4	Project	Planned
Offered Seminar	TUD/AAU	4	Project	Planned
Total ECTS for General Courses = 17				
Total ECTS for Project Courses = 13				
Grand Total = 30				

Tentative Publications

Dresden Database Systems Group

- Demystifying FPGAs.

Aimed Conference: International Workshop on Accelerating Analytics and Data Management Systems Using Modern Processor and Storage Architectures (ADMS).
Submitted Month: June, 2017.

- Implementation and analysis of query processing custom hardware on different types of FPGAs.

Authors: Nusrat Jahan Lisa, Akash Kumar, Torben Bach Pedersen, Wolfgang Lehner.
Aimed Conference: International Workshop on Big Data Management on Emerging Hardware (HardBD).
Expected Submission Month: February, 2018.

- Design an efficient query accelerating bit encoding technique for FPGAs.

Authors: Nusrat Jahan Lisa, Akash Kumar, Torben Bach Pedersen, Wolfgang Lehner
Aimed Conference: International Conference on Extending Database Technology (EDBT).
Expected Submission Month: September, 2018.

- Develop an efficient query accelerating bit encoding technique for modern hardware.

Authors: Nusrat Jahan Lisa, Akash Kumar, Torben Bach Pedersen, Wolfgang Lehner
Aimed Journal: Distributed and Parallel Databases, An International Journal.
Expected Submission Month: March, 2019.